

TMDXEVM6472
Engineering Change Order (ECO)
About RGMII-ID setting of ETH PHY
For PCA REV: 18-00065-01 & 18-00065-02 ONLY
11-JANUARY-2010

Problem Statement

Above versions of board design contains Marvell #88E1121 ethernet PHY (U2). The default board configuration for 88E1121 sets RGMII-Internal Delay timing using CONFIG[3] pin of 88E1121 as “11” meaning both RGMII TX and RX clocks are internally delayed by 88E1121.

This setting may work well for 10/100 Mbps data-rate but it could have an un-reliable RGMII timing when PHY is operated for the data rate of 1000 Mbps. The impact could be an increase in failure rate of ethernet packet delivery at 1000 Mbps data-rate. This could also impact the EMAC boot of C6472 as during network boot-up RGMII EMAC of C6472 operates at 1000 Mbps data-rate.

Solution – Through Hardware resistor soldering

The better RGMII-ID setting at CONFIG[3] pin of 88E1121 should be “01” meaning RGMII TX clock is NOT internally delayed and RGMII RX clock is internally delayed.

Above change can be done by simply changing the assembly of 0E resistors R52 and R53. Resistor R52 should be **mounted(0E)** and resistor R53 should be **un-mounted**.

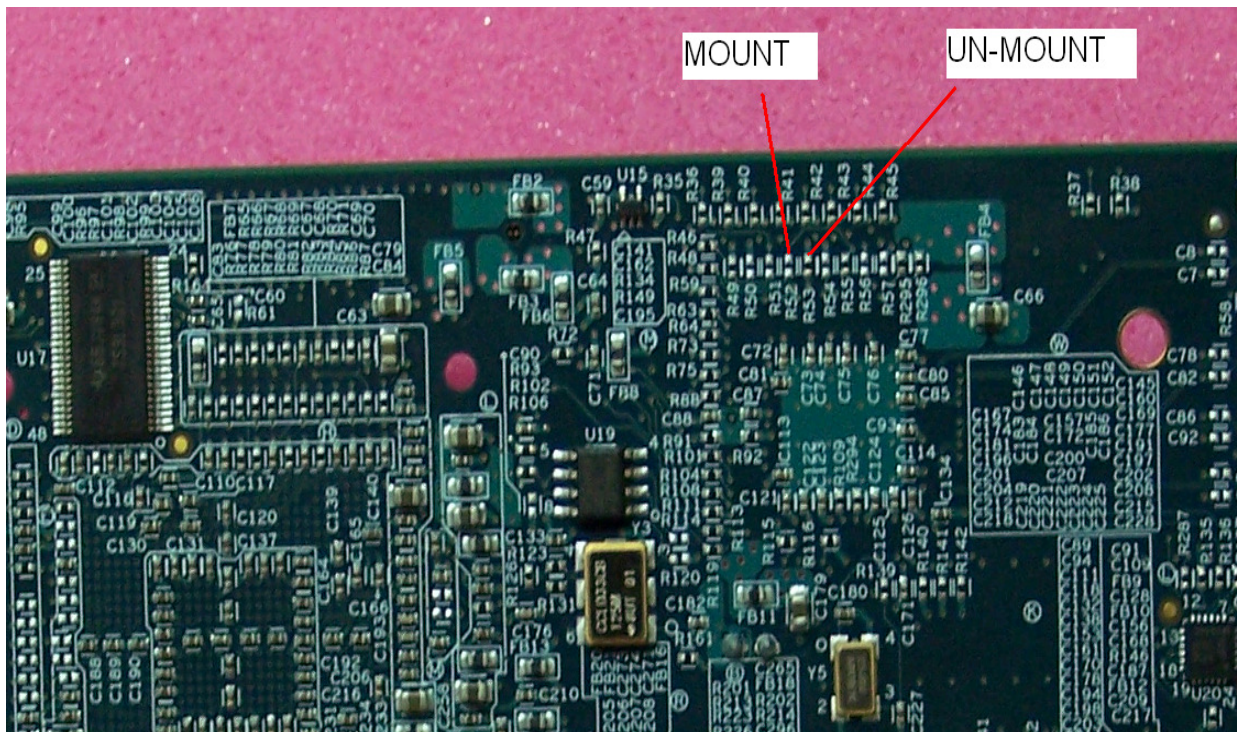


Figure: Position of R52 and R53 – at bottom side of PCB