

C6472EVM Schematics

SCHEMATIC PAGE DESCRIPTION :

- 01 : COVER SHEET
- 02 : SYSTEM BLOCK DIAGRAM
- 03 : DSP - CLOCK, CONFIGURATION, I2C-UART BRIDGE
- 04 : JTAG EMULATION (ON BOARD / EXTERNAL HEADER)
- 05 : DDR2 INTERFACE
- 06 : GIG ETHERNET INTERFACE
- 07 : HPI, TSIP, SRIO INTERFACE, AMC CONNECTOR
- 08 : DSP POWER
- 09 : FPGA - NAND FLASH INTERFACE
- 10 : BOARD POWER SUPPLY & RESET CIRCUITRY
- 11 : REVISION HISTORY & DUMMY PARTS

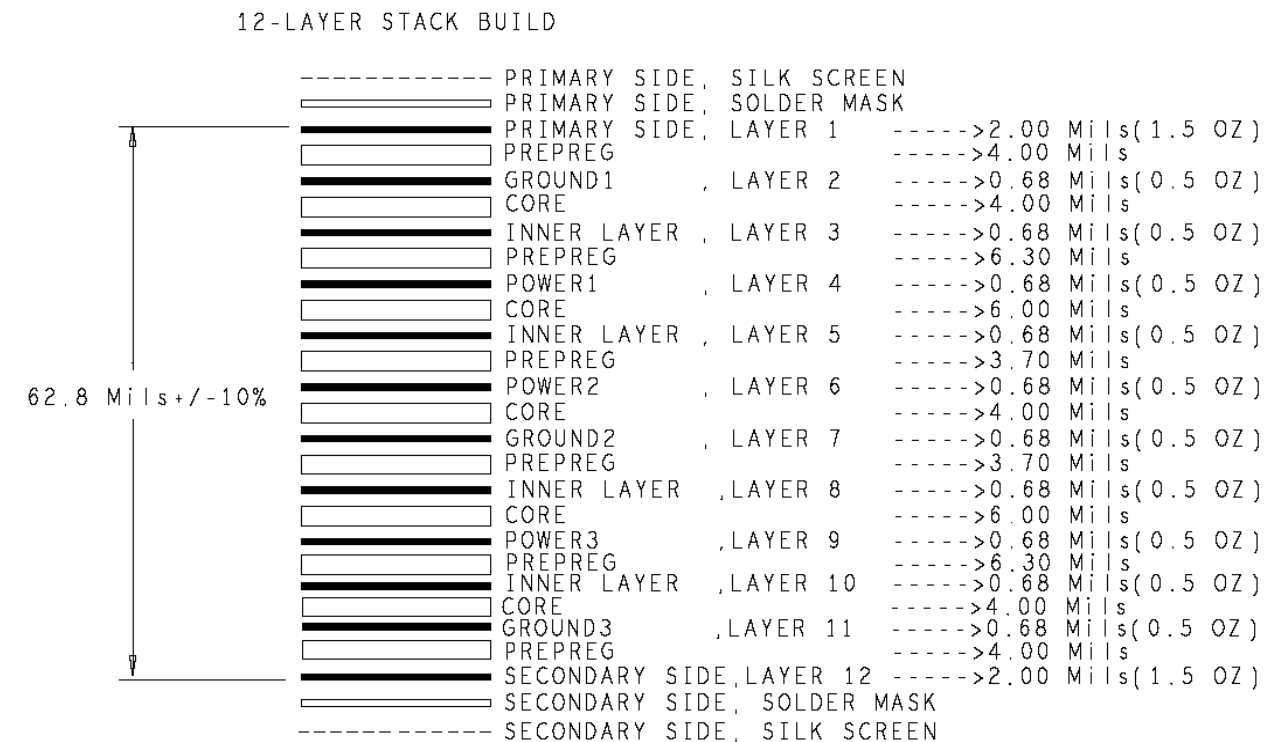
MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	First Build	06-AUGUST-2009
	1.1	First Build - BOM changes	09-SEPTEMBER-2009
2.0	2.0	Second Build - Draft	21-SEPTEMBER-2009
	2.1	Second Build - Release	24-SEPTEMBER-2009

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
U19	I2C EEPROM	0x50
U20	I2C - UART BRIDGE	0x4D
J2	AMC CONNECTOR	TBD
U9	FPGA	TBD
U25	I2C - I/O EXPANDER	0x41

PCB LAYER STACK-UP DETAILS :



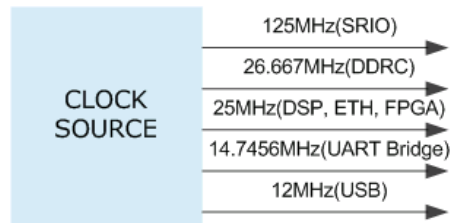
PCB Mechanical Details :

- PCB SIZE: 7.11" x 2.89" x 0.063"
- PCB MATERIAL: FR4
- NUMBER OF LAYERS: 12
- IMPEDANCE CONTROL: YES

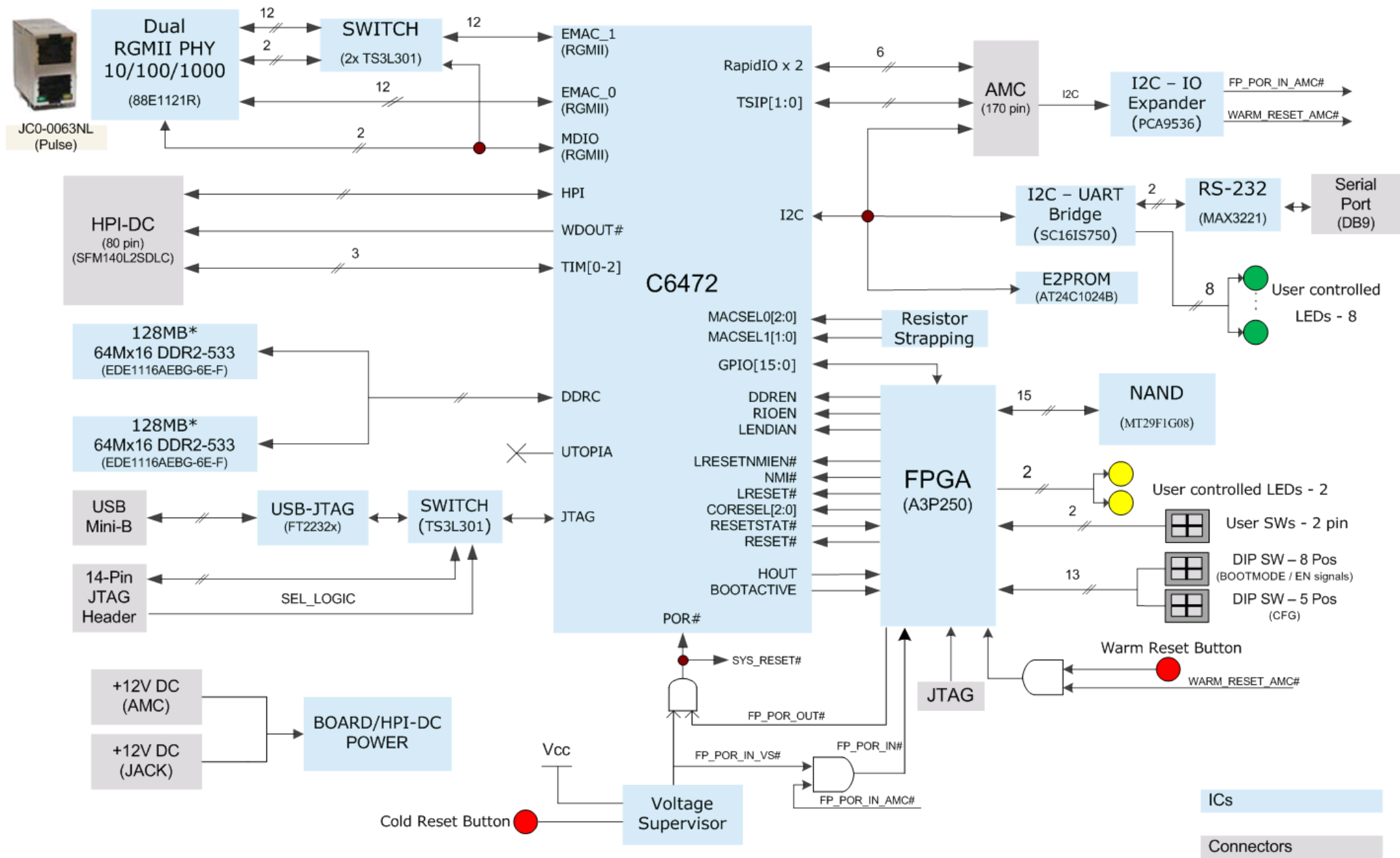
NOTES, UNLESS OTHERWISE SPECIFIED :

- RESISTANCE VALUES ARE IN OHMS.
- CAPACITANCE VALUES ARE IN MICROFARADS.
- PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
- SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

Project TI_C6472EVM		Designed for TI by eInfochips	
Title Cover Sheet			
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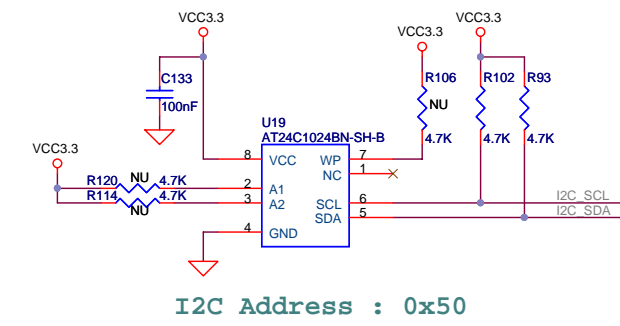
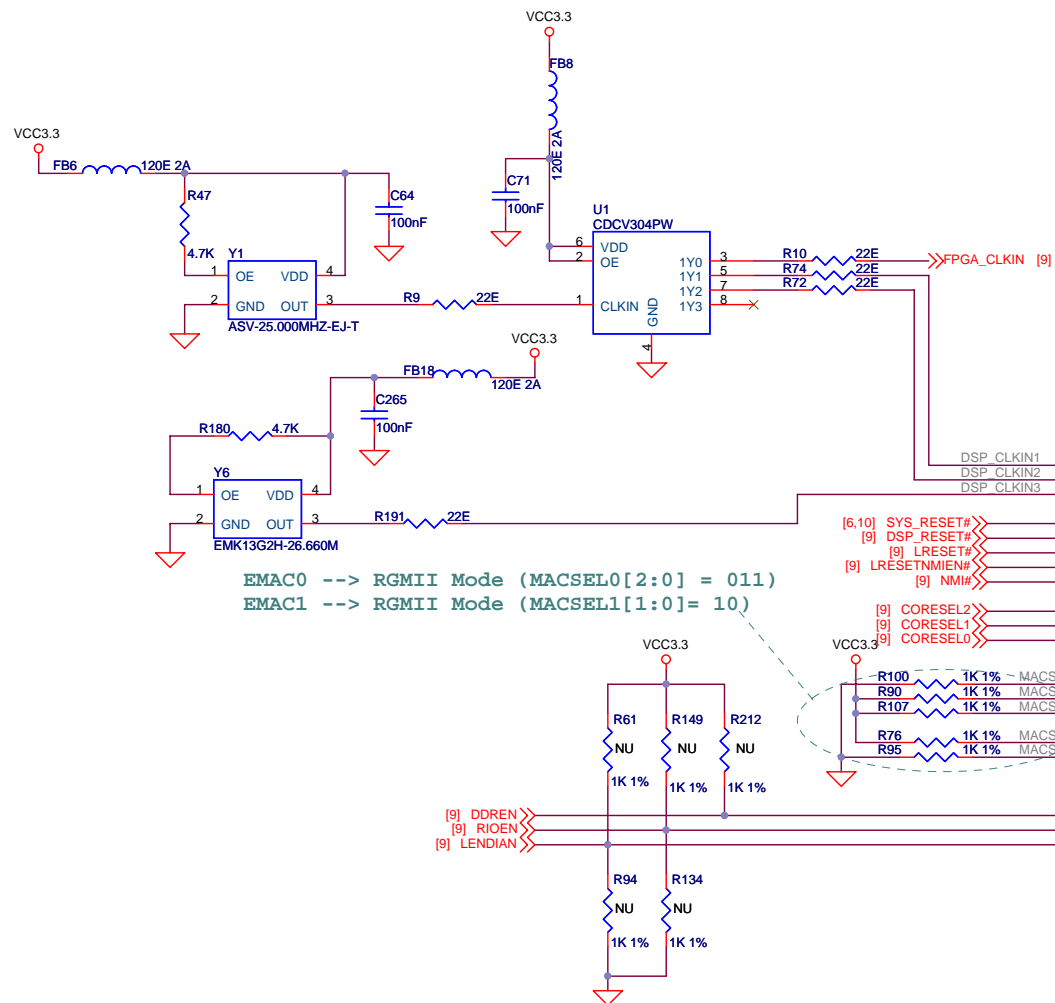
BLOCK DIAGRAM



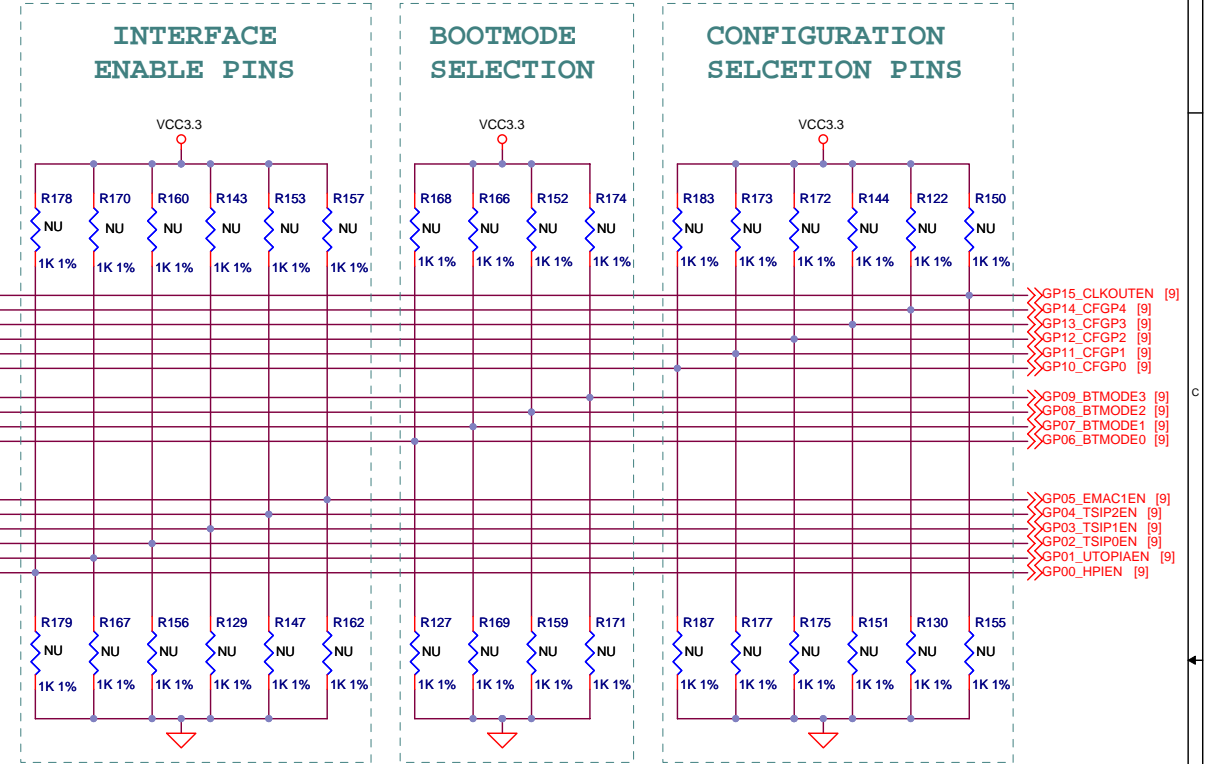
Notes:

- 1) GPIO[15:0] are multiplexed with configuration pins
- 2) *RAM expandable to 512MB(128Mx16) DDR2-533

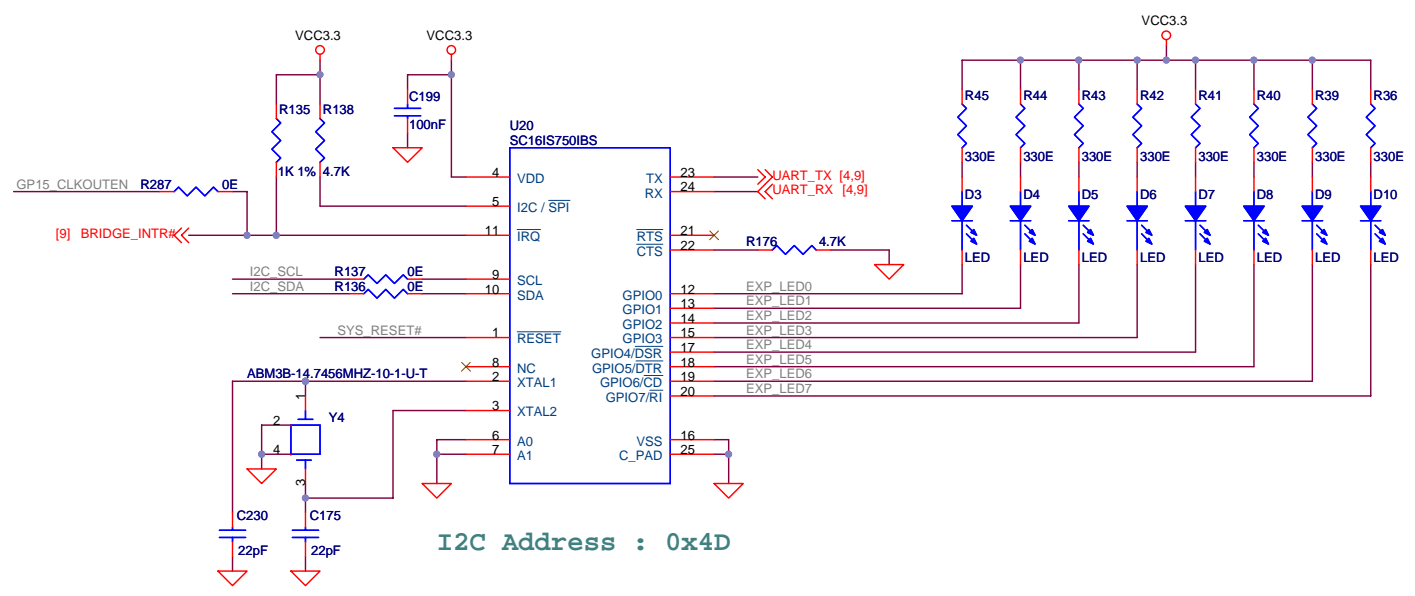
Project TI_C6472EVM		Designed for TI by elnfochips	
Title System Block Diagram			
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FPGA to drive GP[15:00], DDREN, RIOEN & LENDIAN signals at reset



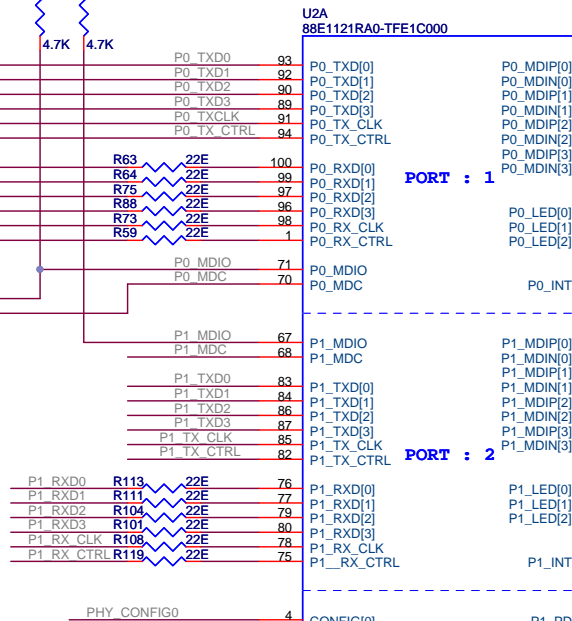
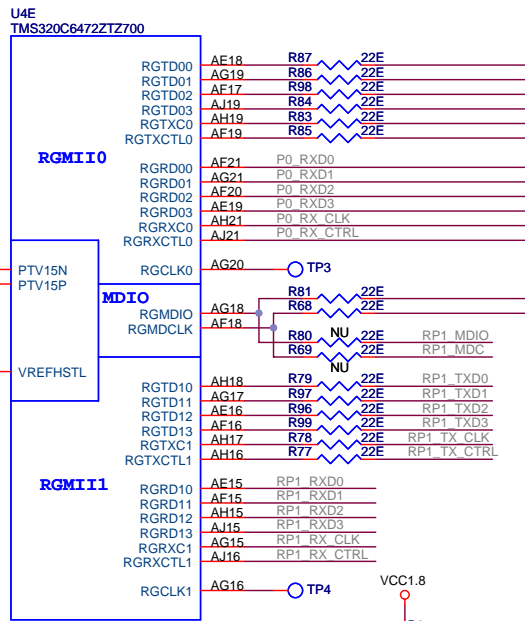
I2C - UART Bridge



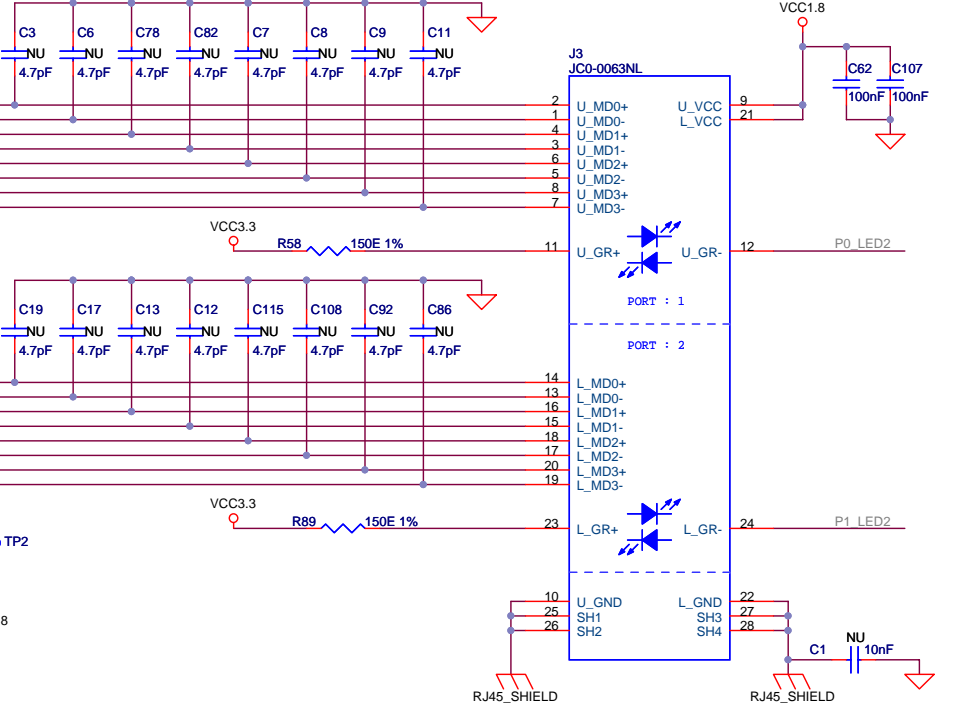
BOOTMODE[3:0]	DESCRIPTION
0000 (0)	Immediate Boot
0001 (1)	Host (HPI) boot
0010 (2)	Master I2C boot (address : 50H) -- Default
0011 (3)	Master I2C boot (address : 51H)
0100 (4)	Slave I2C boot
0101 (5) - 1000 (8)	UTOPIA boot
1001 (9)	EMAC0 boot
1010 (10)	EMAC1 boot
1011 (11) - 1110 (14)	RIO[1:4]
1111 (15)	Reserved

Project TI_C6472EVM		Designed for TI by elnfochips	
Title DSP Configuration, UART Bridge			
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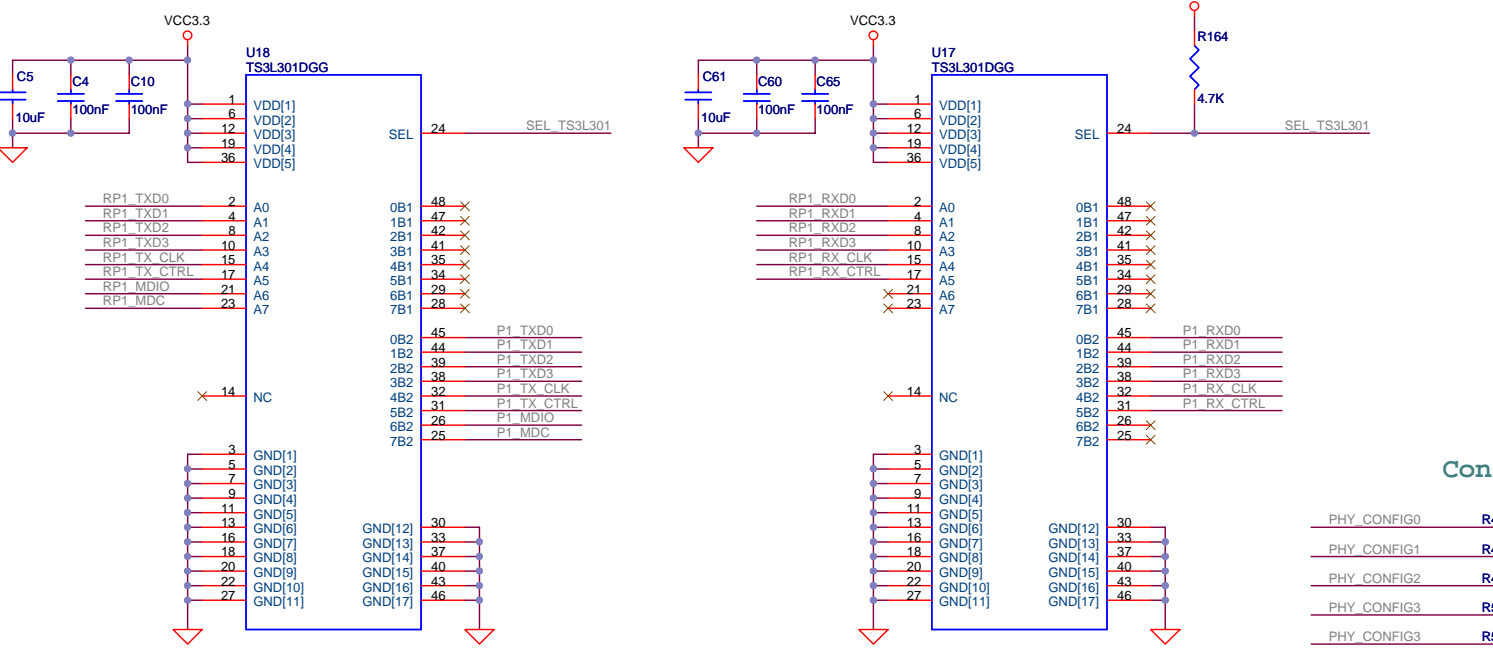
C6472 Ethernet MAC (RGMII)



Dual Port GiG Ethernet PHY



Dual Port Connector



Switch for Ethernet Port # 1

AMC_ENABLE# (SEL) = 0 --> EMAC1 = To AMC connector
 AMC_ENABLE# (SEL) = 1 --> EMAC1 = To 88E1121 PHY

Port 0 Address : 11000
 Port 1 Address : 11001

Configuration

PHY_CONFIG0	R48	0E	"00"
PHY_CONFIG1	R49	0E	"11"
PHY_CONFIG2	R46	0E	P0_LED1
PHY_CONFIG3	R51	NU	0E
PHY_CONFIG3	R52	NU	0E
PHY_CONFIG3	R50	NU	0E
PHY_CONFIG3	R53	0E	"11"
PHY_CONFIG4	R8	0E	"11"
PHY_CONFIG5	R56	0E	P0_LED1
PHY_CONFIG5	R55	NU	0E
PHY_CONFIG5	R57	NU	0E
PHY_CONFIG5	R54	0E	"11"

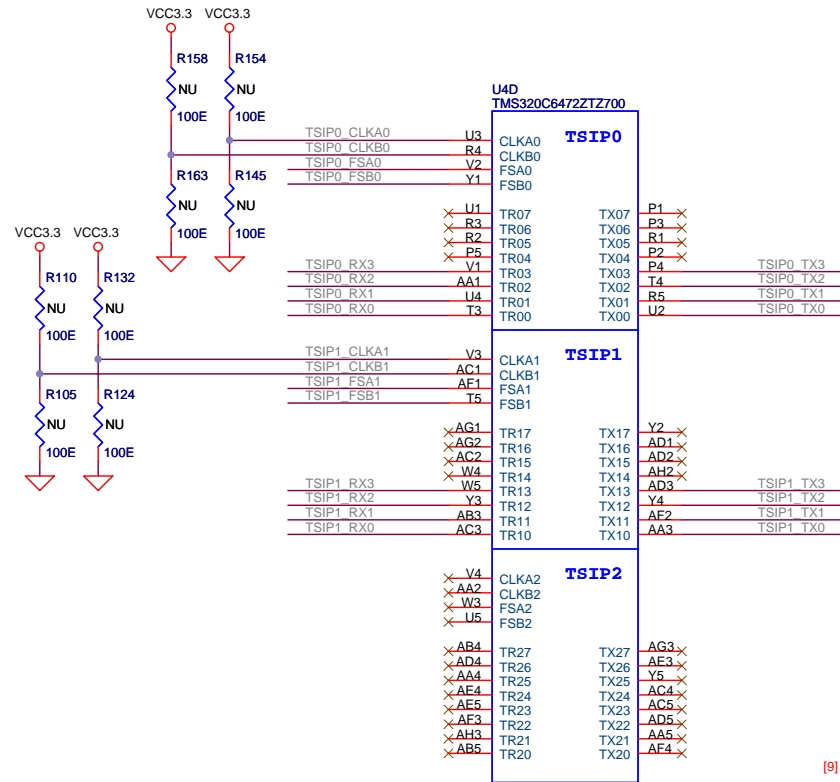
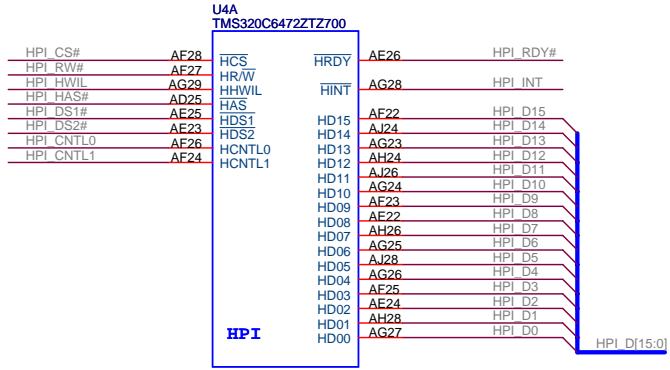
TWO Pin Mapping

Pin	Bit 1,0
VSS	00
Px_LED[0]	01
Px_LED[1]	10
VDDO	11

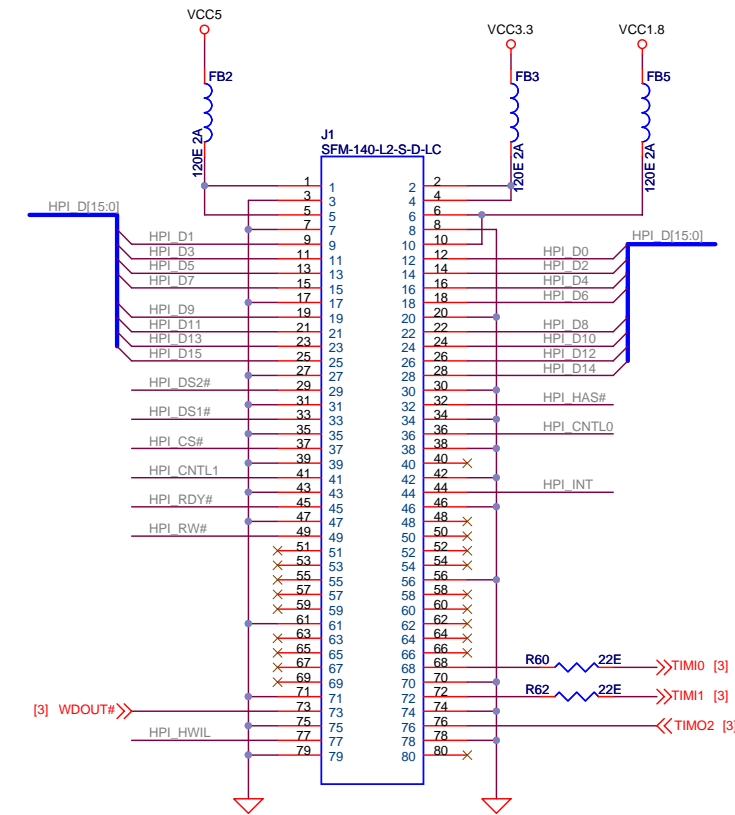
Project TI_C6472EVM		Designed for TI by eInfochips	
Title GiG Ethernet Interface			
Size C	Document Number 16-0065-02	Rev 2.1	
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Note: Auto cross over functionality is enabled

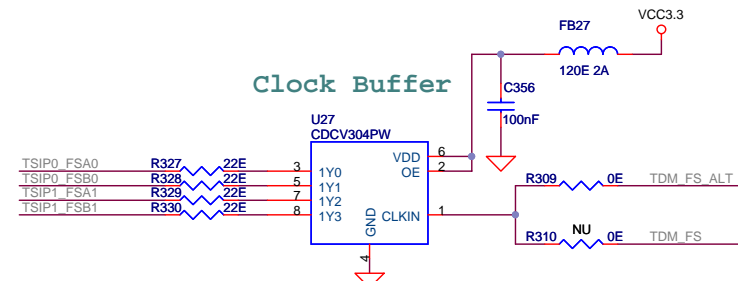
C6472 HPI Interface



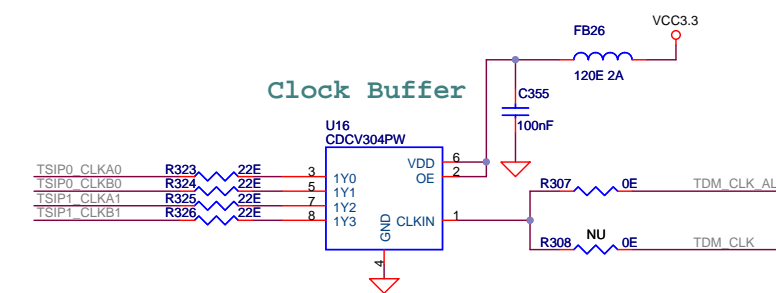
TSIP Interface



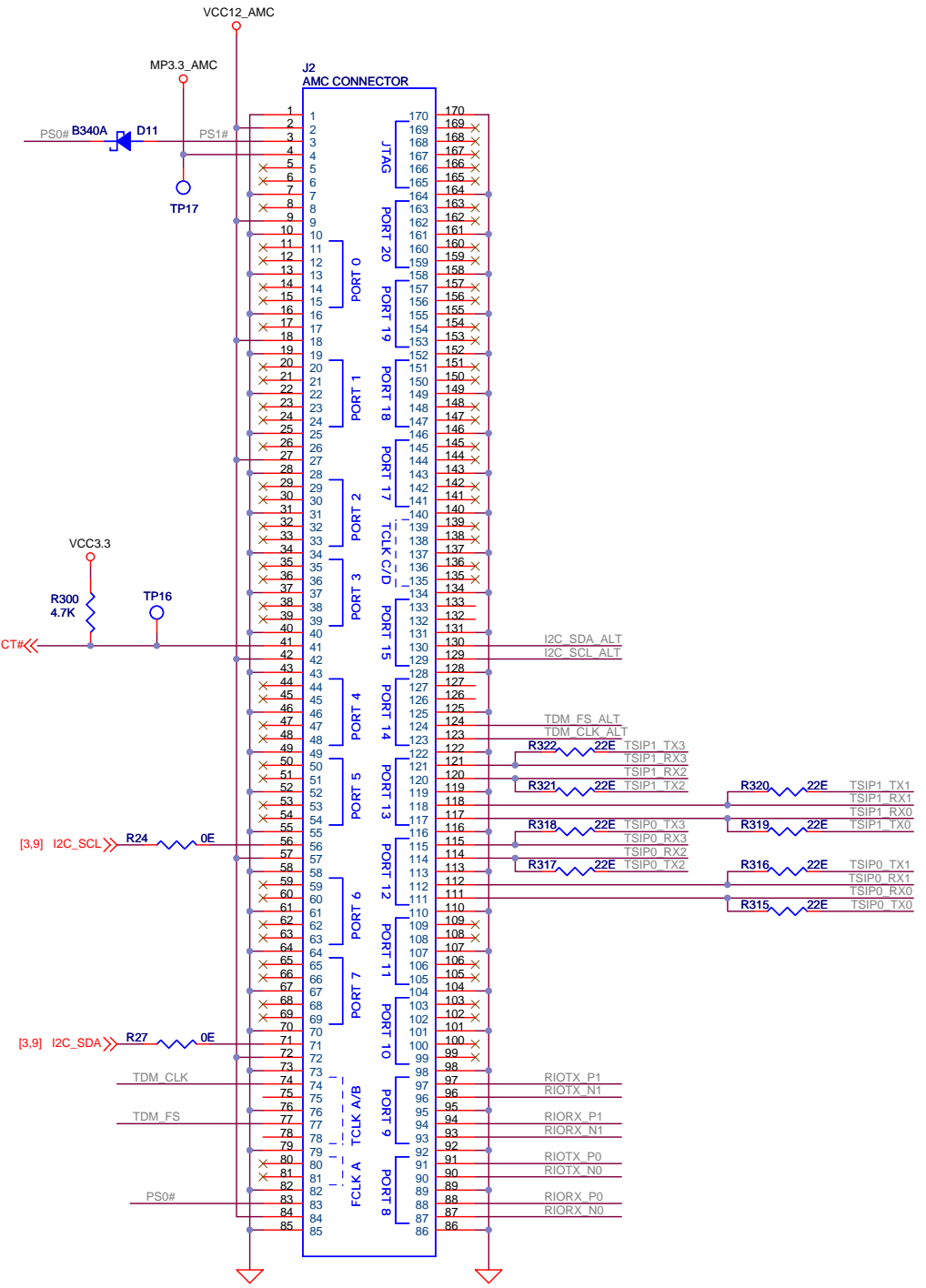
HPI DC Connector



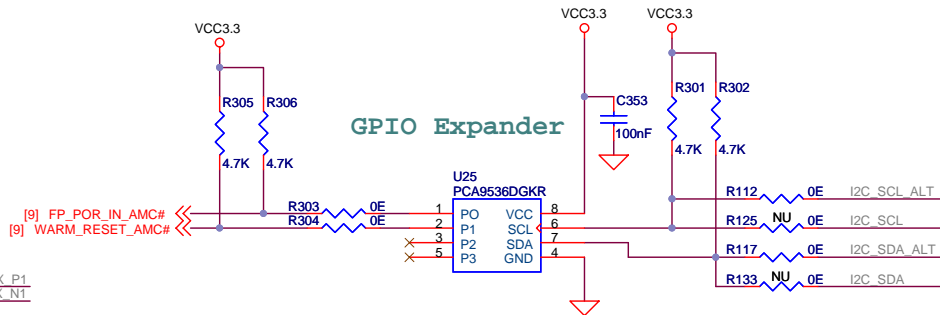
Clock Buffer



Clock Buffer

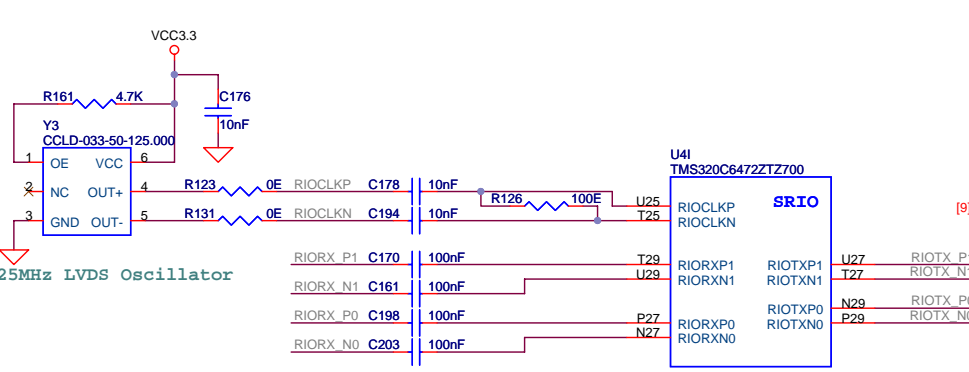


AMC Connector



GPIO Expander

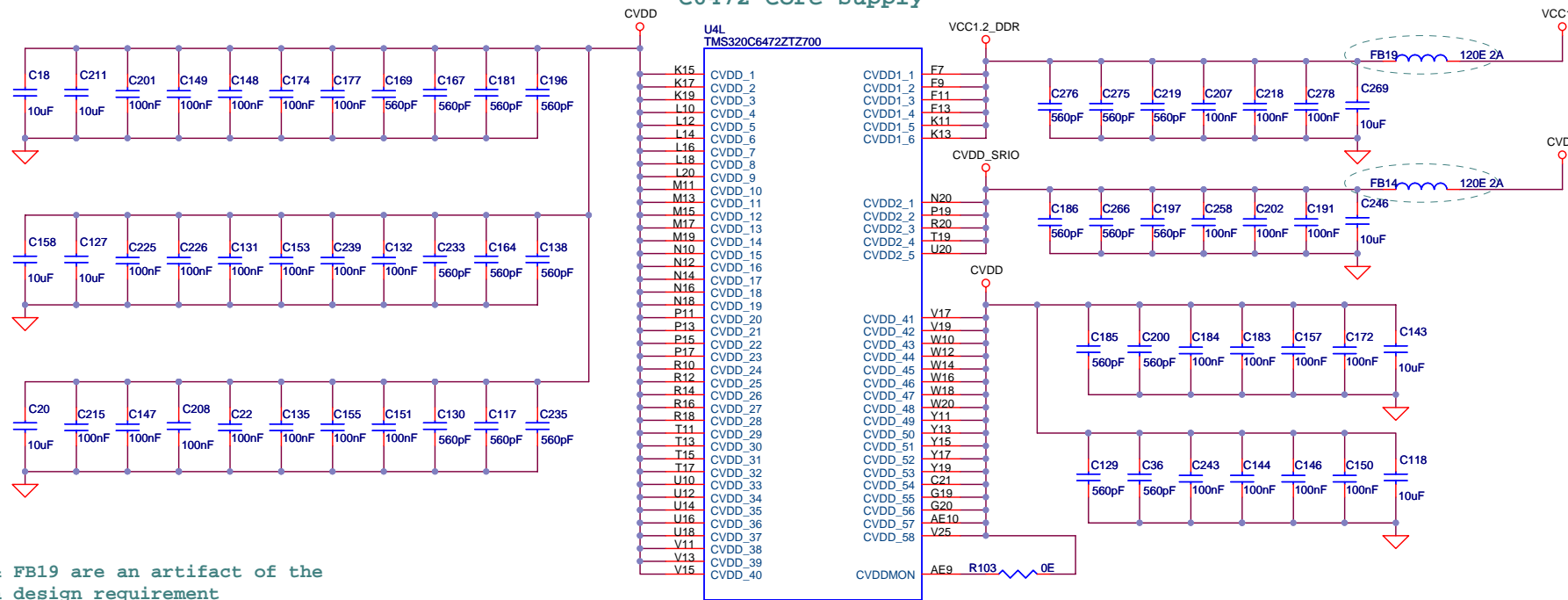
I2C Address : 0x41



C6472 SRIO Interface

Project TI_C6472EVM		Designed for TI by eInfochips	
Title HPI, AMC Connector Interface			
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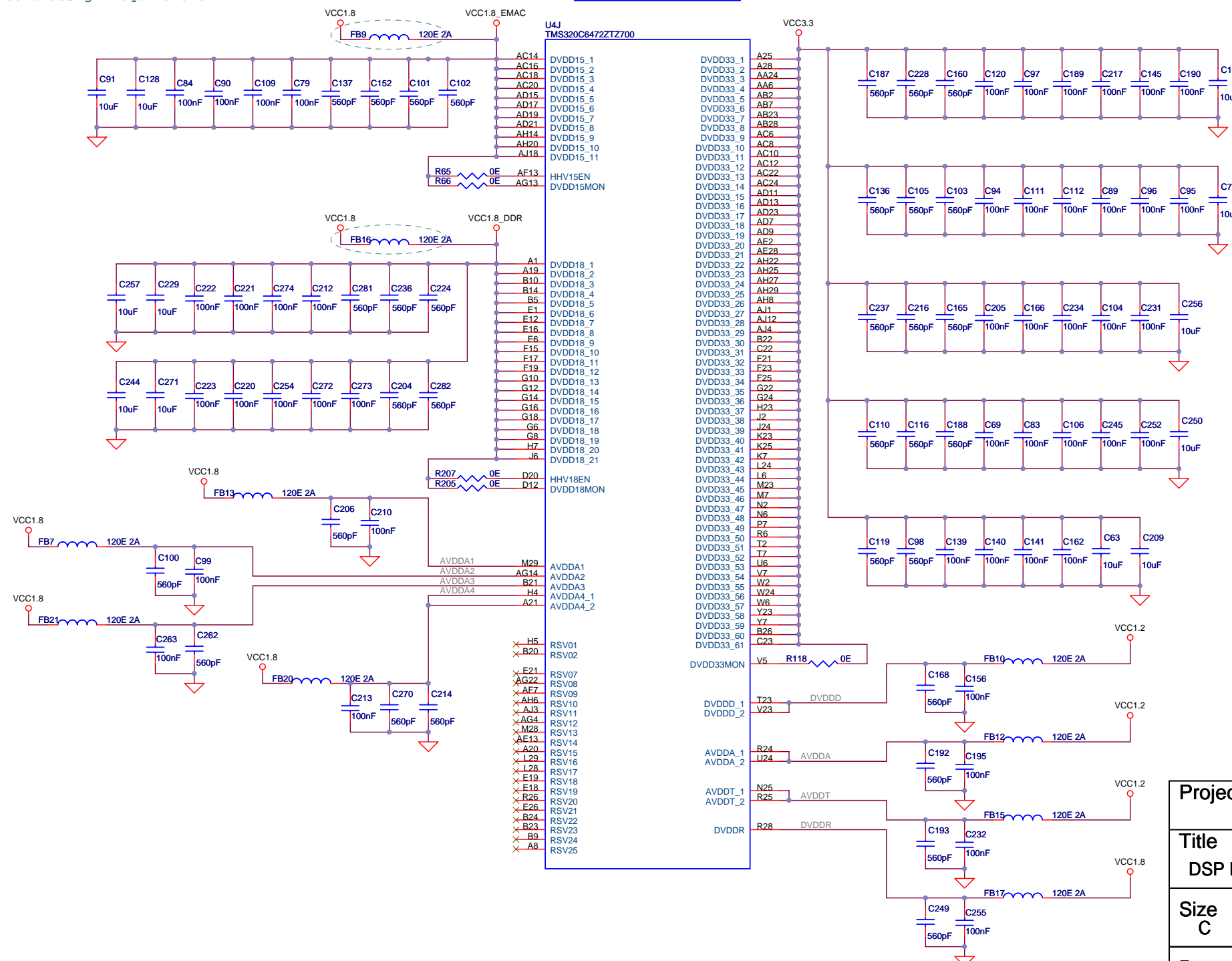
C6472 Core Supply



FB9, FB14, FB16 & FB19 are an artifact of the EVM design, not a design requirement

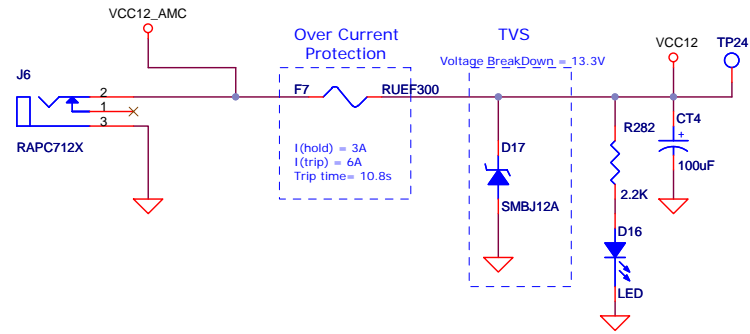
U4K TMS320C6472ZT700			
A10	VSS1	VSS91	Y6
A14	VSS2	VSS92	Y24
A18	VSS3	VSS93	Y20
A2	VSS4	VSS94	Y18
A22	VSS5	VSS95	Y16
A26	VSS6	VSS96	Y14
A30	VSS7	VSS97	Y12
AA23	VSS8	VSS98	Y10
AA7	VSS9	VSS99	W7
AB1	VSS10	VSS100	W23
AB5	VSS11	VSS101	W19
AB9	VSS12	VSS102	W17
AB13	VSS13	VSS103	W15
AB17	VSS14	VSS104	W13
AB21	VSS15	VSS105	W11
AC11	VSS16	VSS106	W1
AC15	VSS17	VSS107	W6
AC19	VSS18	VSS108	W2
AC23	VSS19	VSS109	W24
AC27	VSS20	VSS110	W20
AC31	VSS21	VSS111	W18
AC35	VSS22	VSS112	W16
AD10	VSS23	VSS113	V14
AD14	VSS24	VSS114	V12
AD18	VSS25	VSS115	V10
AD22	VSS26	VSS116	U28
AD26	VSS27	VSS117	U24
AD30	VSS28	VSS118	U22
AD34	VSS29	VSS119	U20
AD38	VSS30	VSS120	U17
AD42	VSS31	VSS121	U15
AE1	VSS32	VSS122	U11
AE5	VSS33	VSS123	T6
AE9	VSS34	VSS124	T8
AE13	VSS35	VSS125	T2
AE17	VSS36	VSS126	T4
AE21	VSS37	VSS127	T20
AE25	VSS38	VSS128	T18
AE29	VSS39	VSS129	T16
AE33	VSS40	VSS130	T14
AE37	VSS41	VSS131	T12
AE41	VSS42	VSS132	T10
AE45	VSS43	VSS133	T1
AE49	VSS44	VSS134	R7
AE53	VSS45	VSS135	R23
AE57	VSS46	VSS136	R19
AE61	VSS47	VSS137	R17
AE65	VSS48	VSS138	R15
AE69	VSS49	VSS139	R13
AE73	VSS50	VSS140	R11
AE77	VSS51	VSS141	P6
AE81	VSS52	VSS142	P8
AE85	VSS53	VSS143	P4
AE89	VSS54	VSS144	P2
AE93	VSS55	VSS145	P26
AE97	VSS56	VSS146	P22
AE101	VSS57	VSS147	P24
AE105	VSS58	VSS148	P20
AE109	VSS59	VSS149	P18
AE113	VSS60	VSS150	P16
AE117	VSS61	VSS151	P14
AE121	VSS62	VSS152	P12
AE125	VSS63	VSS153	P10
AE129	VSS64	VSS154	M7
AE133	VSS65	VSS155	M23
AE137	VSS66	VSS156	M19
AE141	VSS67	VSS157	M17
AE145	VSS68	VSS158	M15
AE149	VSS69	VSS159	M13
AE153	VSS70	VSS160	M11
AE157	VSS71	VSS161	M9
AE161	VSS72	VSS162	M7
AE165	VSS73	VSS163	M5
AE169	VSS74	VSS164	M3
AE173	VSS75	VSS165	M1
AE177	VSS76	VSS166	M27
AE181	VSS77	VSS167	M23
AE185	VSS78	VSS168	M19
AE189	VSS79	VSS169	M17
AE193	VSS80	VSS170	M15
AE197	VSS81	VSS171	M13
AE201	VSS82	VSS172	M11
AE205	VSS83	VSS173	M9
AE209	VSS84	VSS174	M7
AE213	VSS85	VSS175	M5
AE217	VSS86	VSS176	M3
AE221	VSS87	VSS177	M1
AE225	VSS88	VSS178	L17
AE229	VSS89	VSS179	L15
AE233	VSS90	VSS180	L13
AE237	VSS91	VSS181	L11
AE241	VSS92	VSS182	AJ23
AE245	VSS93	VSS183	D21
AE249	VSS94	VSS184	D18

C6472 Ground

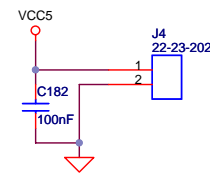


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Title DSP Power Supply			
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12V DC Input Supply



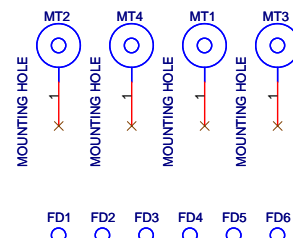
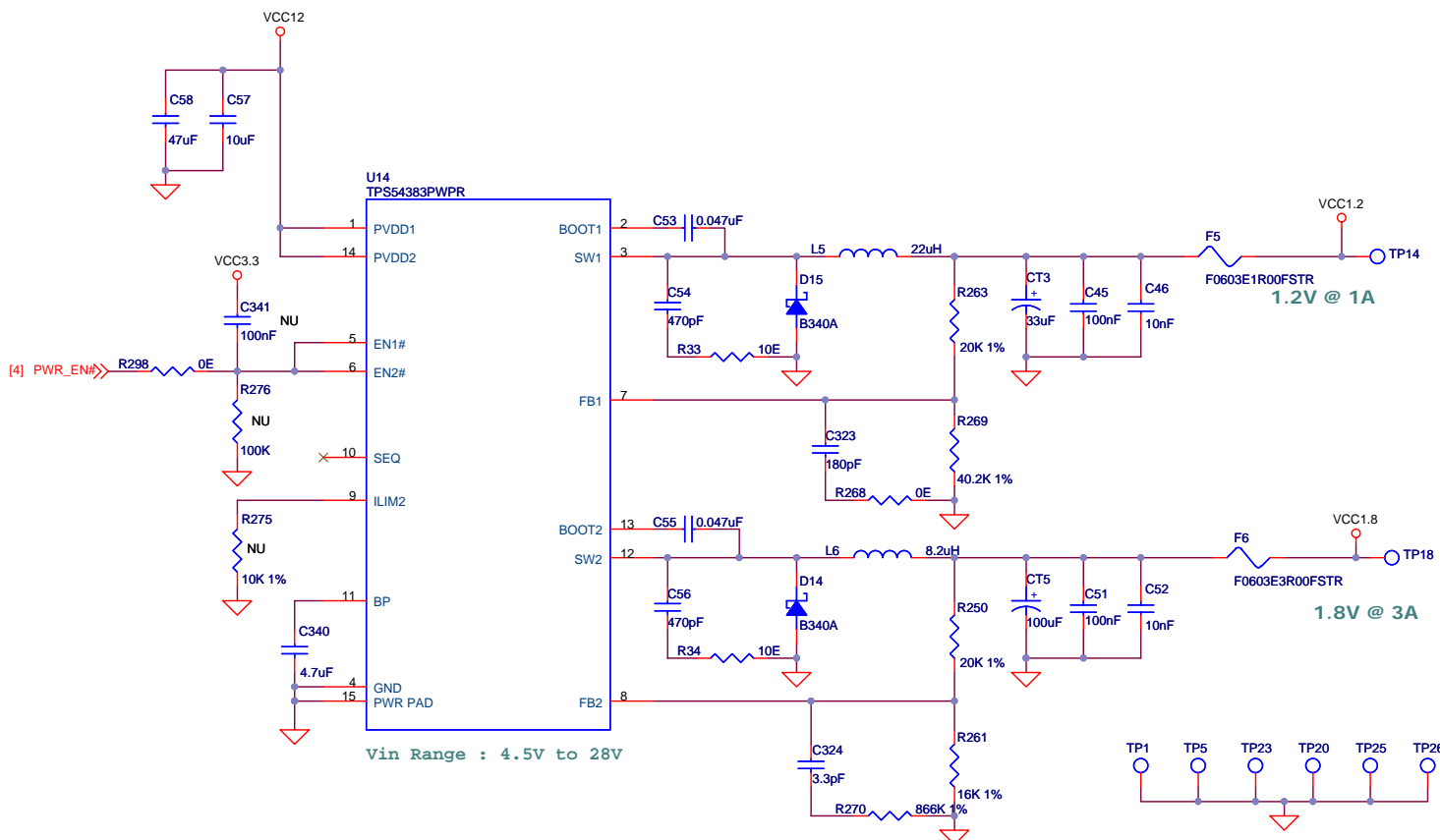
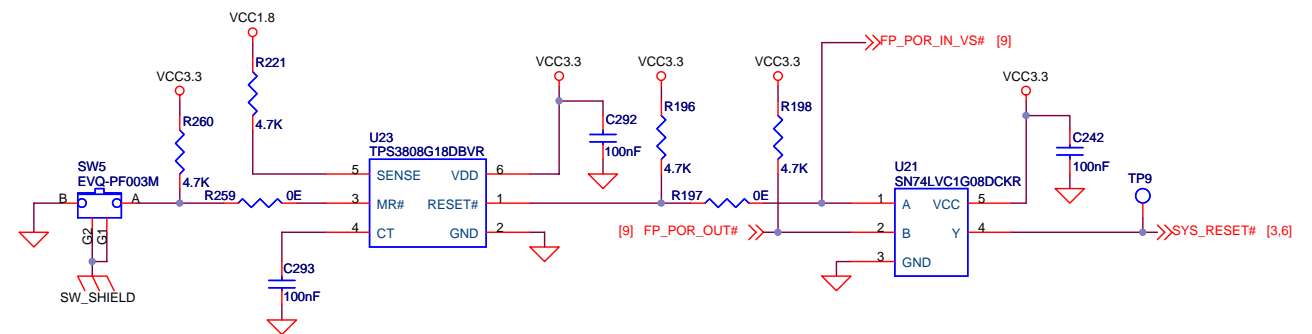
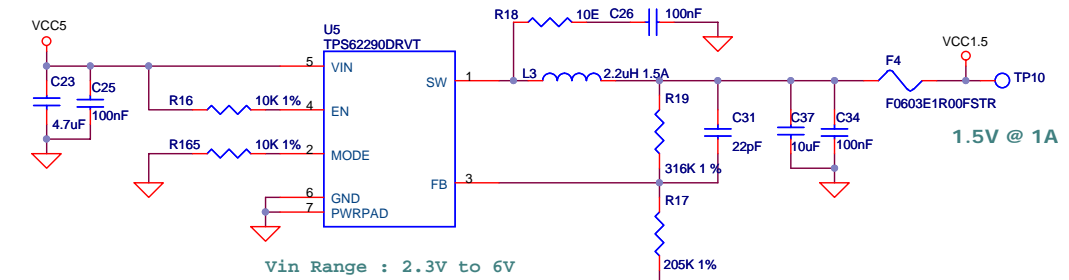
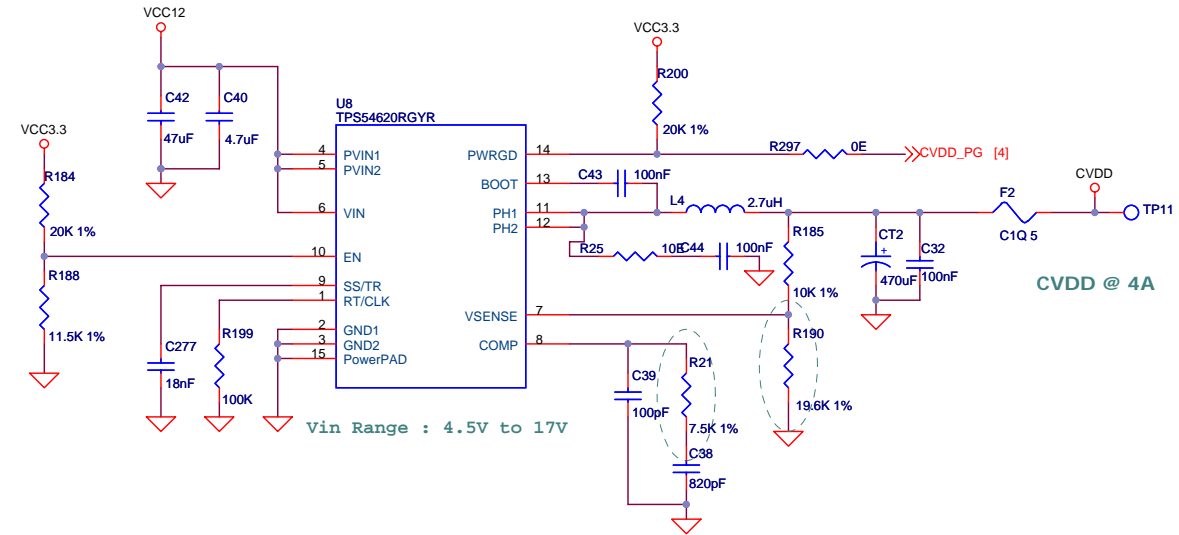
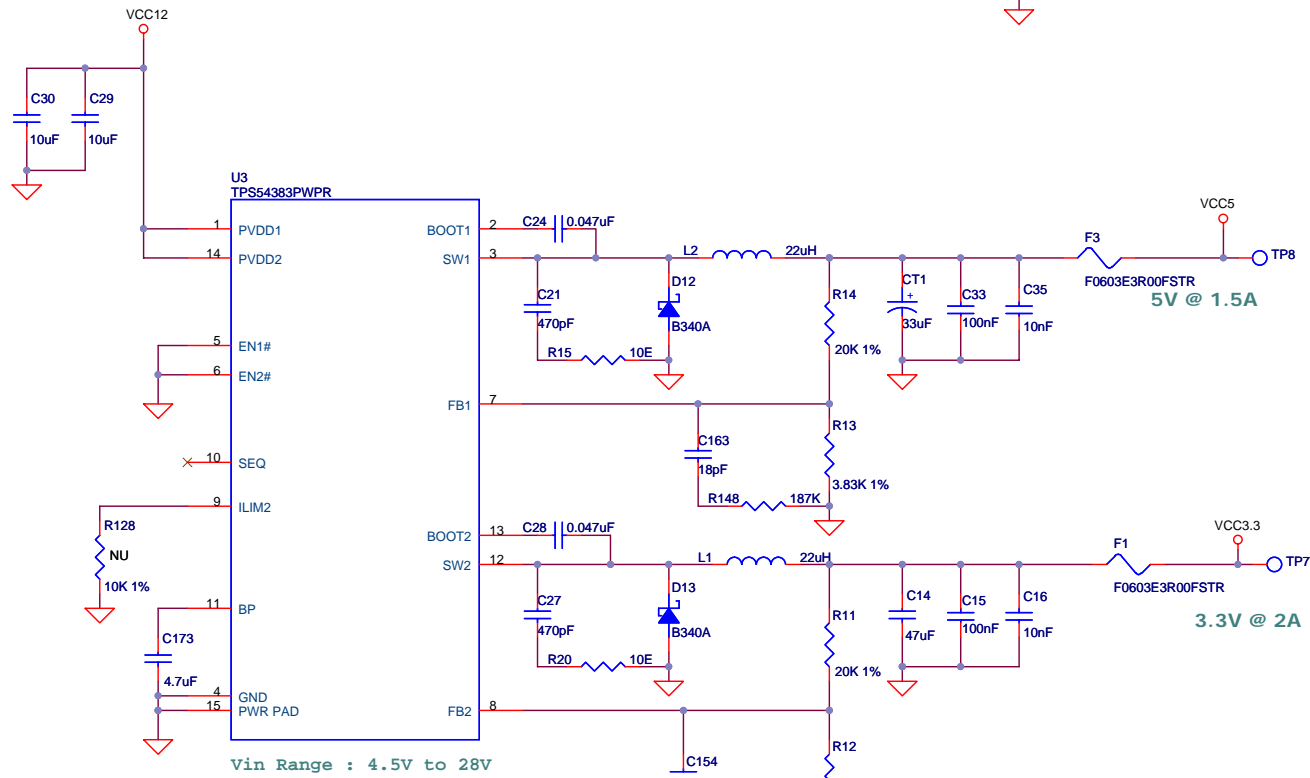
5V DC for FAN



CVDD Three Options:

Board will support three options for CVDD voltage generation to have Frequency support of 500MHz, 625MHz & 700MHz

	CVDD - 1V (500MHz)	CVDD - 1.1V (625MHz)	CVDD - 1.2V (700MHz)
R190	38.3K 1%	26.1K 1%	19.6K 1%
R21	6.19K 1%	6.81K 1%	7.5K 1%

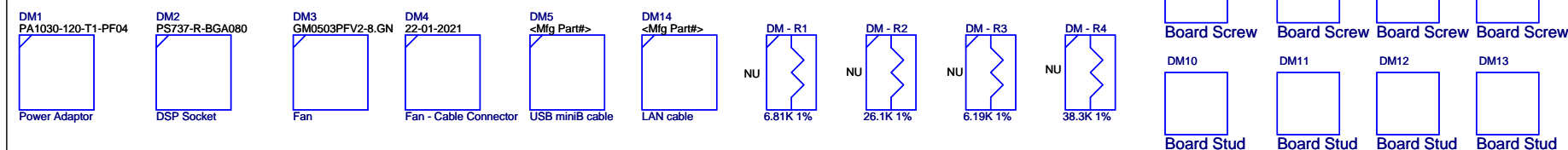


Project TI_C6472EVM		Designed for TI by eInfochips	
Title Board Power Supply			
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TI_C6472EVM - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	Draft 0.1	- Initial draft is created	26JUN2009	eInfochips
	Draft 0.2	- Following interfaces added : - DSP Configurations, SRIO, TSIP, HPI, FPGA	01JUL2009	eInfochips
	Draft 0.3	- BOM attributes added - Modifications after Internal review	06JUL2009	eInfochips
	Draft 0.4	- Input Power changed from 12V to 5V (TPS5450 & related circuitry removed, AMC payload power is changed to 5V) - To support 700MHz frequency, Two inputs are given to FPGA to have total 3 combinations - ESD protection added & 33E Resistor, 47pF Capacitors removed on USB lines for JTAG emulation (As per comments by FTDI expert reviewer) - UART signals taken on FTDI chip - Crystals' part # changed - Parallel terminations added on TSIP clock lines - DSP Pulled UP / Pulled DOWN value changed to 1K, as per datasheet recommendation - Modifications after TI review on 10-July - Aesthetical changes	14JUL2009	eInfochips
	Draft 0.5	- DDR2 data lines & FPGA IOs are swapped for ease of routing - Input voltage changed to 12V (TPS54383 added for 12 to 5V & 3.3V generation, removing TPS54356 for 5 to 3.3V generation) - Reset logic changed - FPGA net names changed for better understanding of pin mapping - Two 25MHz oscillators removed & one clock buffer added - Re-sequencing performed	22JUL2009	eInfochips
	Draft 0.6	- U14 Enable logic changed - Seperate Pull Up provided on pin # 21, 22 & 24 of PHY - Modified AMC pin outs - SRIO, TSIP0, TSIP1 pin outs changed, TSIP2 & RGMII removed (Removed TL3LG switches)	29JUL2009	eInfochips
	Issue 1.0	- Released for Fabrication of PCB ver1.0 (Proto-1)	06AUG2009	eInfochips
	Issue 1.1	- Page # 6 : Mounting Status of R55, R58, R89, R69 & R80 is changed to NU & R56 is changed to Used - Updated BOM for second batch of 22 boards	09SEP2009	eInfochips
2.0	Draft 2.0	- R126 shifted to DSP side - Values of R21 and R190 set for CVDD=1.2V - Designed Eth PHY for single LED - Low Active - Green Color using LED[2] signal from both Ethernet ports. Values of R58 and R89 changed to 150E and driven from VCC3.3, Mounting status of R58 and R89 changed to "Used". - Added GPIO expander U25 on AMC I2C line to control reset from a AMC host - Added dual AND gate U26 on FPGA POR and warm reset to have reset control from AMC host board - Added clock buffers for TSIP - CLK and FS - AMC Port TCLKA&B used for TDM_CLK/TDM_FS, AMC Port 12 used for TDM[3:0], AMC Port 13 used for TDM[7:4] - AMC Port 14 used for Alternate TDM_CLK/TDM_FS, AMC Port 15 used for alternate I2C - AMC Port TCLKC&D, Port 17, Port 18, Port 19 and Port 20 changed to not used - USB miniB cable added as Dummy part - Mounting status of R14 and R26 changed to Used from "Not-Used(NU)", For Board build ID feature addition.	21SEP2009	eInfochips
	Issue 2.1	- Pull-up resistors R301 and R302 moved to the inputs side of U25, C293 changed to 100nF, C352 added on Warm Reset line.	24SEP2009	eInfochips

Dummy Components



Project TI_C6472EVM		Designed for TI by eInfochips	
Title Revision History & Dummy Parts			
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