C6472EVM Schematics

SCHEMATIC PAGE DESCRIPTION :

01 : COVER SHEET
02 : SYSTEM BLOCK DIAGRAM
03 : DSP - CLOCK, CONFIGURATION, I2C-UART BRIDGE
04 : JTAG EMULATION (ON BOARD / EXTERNAL HEADER)
05 : DDR2 INTERFACE
06 : GIG ETHERNET INTERFACE_1
07 : GIG ETHERNET INTERFACE_2
08 : TSIP, SRIO INTERFACE, MMC, AMC CONNECTOR
09 : HPI INTERFACE, DSP POWER
10 : FPGA - NAND FLASH INTERFACE
11 : BOARD POWER SUPPLY & RESET CIRCUITRY
12 : REVISION HISTORY & DUMMY PARTS

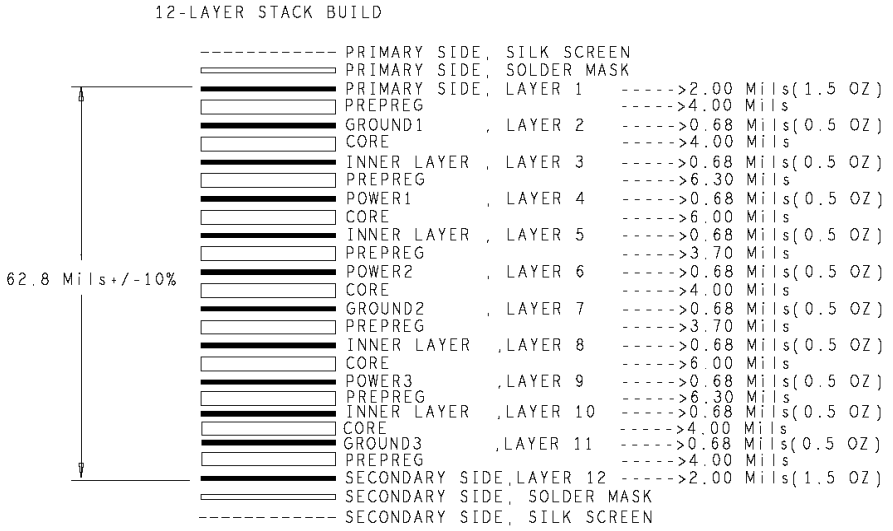
MAJOR REVISION HISTORY :

PCB REV.	SCH. REV.	DESCRIPTION	DATE
1.0	1.0	First Build (Alpha)	06-AUGUST-2009
	1.1	First Build (Beta)	09-SEPTEMBER-2009
2.0	2.1	Second Build (AMC/TSIP/I2C chagnes)	24-SEPTEMBER-2009
3.0	3.2	SGMII feature addition proto Build	27-OCTOBER-2009
4.0	4.2	SGMII Production Build (PHY configuration changes)	22-JANUARY-2010
5.0	5.3	IPMI and XDS560v2 support added	12-JULY-2010
6.0	6.0	TCLKC/D used for Frame Sync	04-SEPTEMBER-2010
	6.1	D18 par# changed	19-NOVEMBER-2010

I2C ADDRESS TABLE :

REF DES	DESCRIPTION	7 BIT ADDRESS
U19	I2C EEPROM	0x50
U20	I2C - UART BRIDGE	0x4D
U9	FPGA	TBD

PCB LAYER STACK-UP DETAILS :



PCB Mechanical Details :

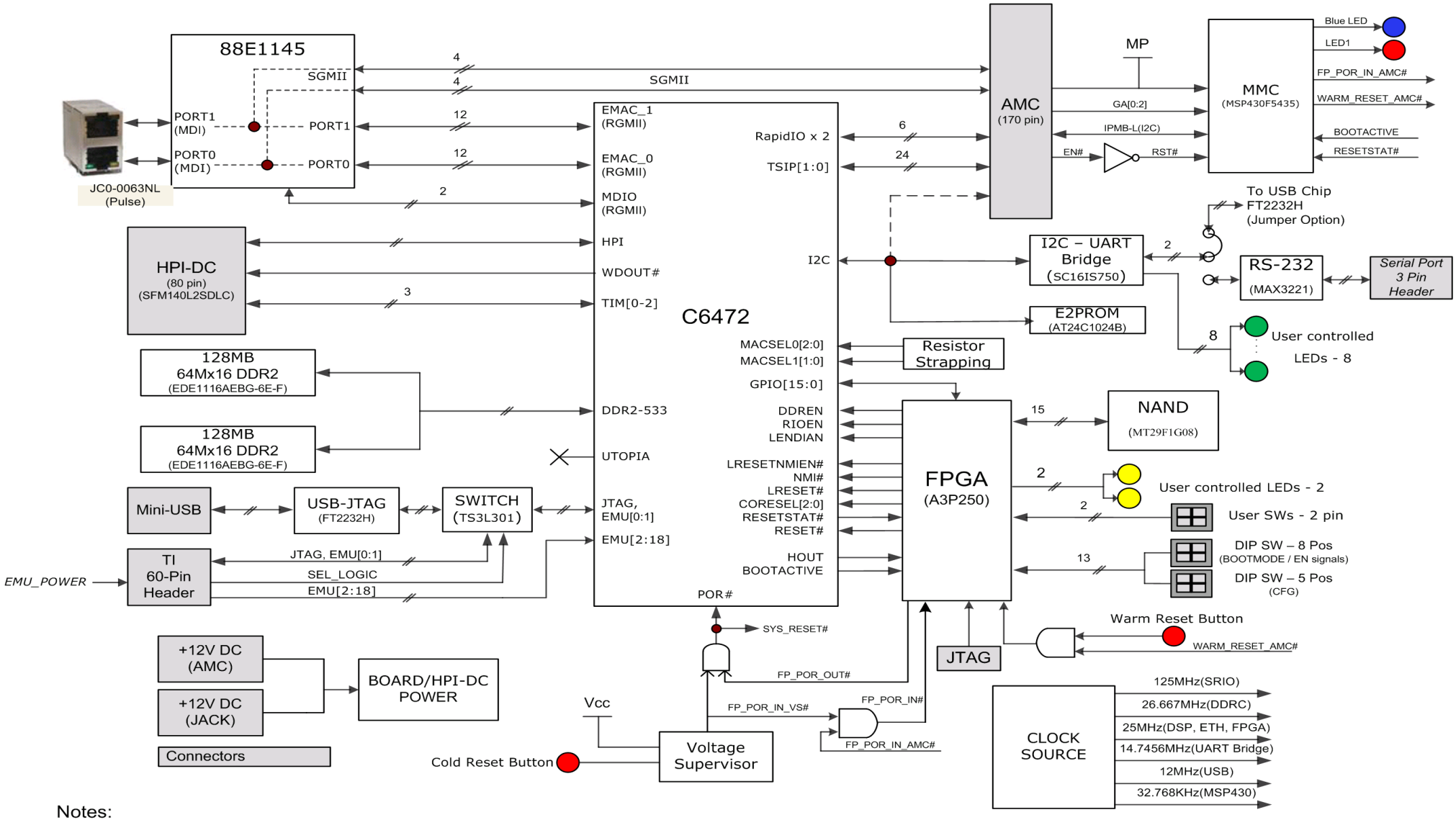
1. PCB SIZE: 7.11" x 2.89" x 0.063"
2. PCB MATERIAL: FR4
3. NUMBER OF LAYERS: 12
4. IMPEDANCE CONTROL: YES

NOTES, UNLESS OTHERWISE SPECIFIED :

1. RESISTANCE VALUES ARE IN OHMS.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. PARTS NOT INSTALLED ARE INDICATED WITH 'NU'.
4. SIGNAL NET NAMES WITH "#" SUFFIX, ARE ACTIVE LOW SIGNALS.

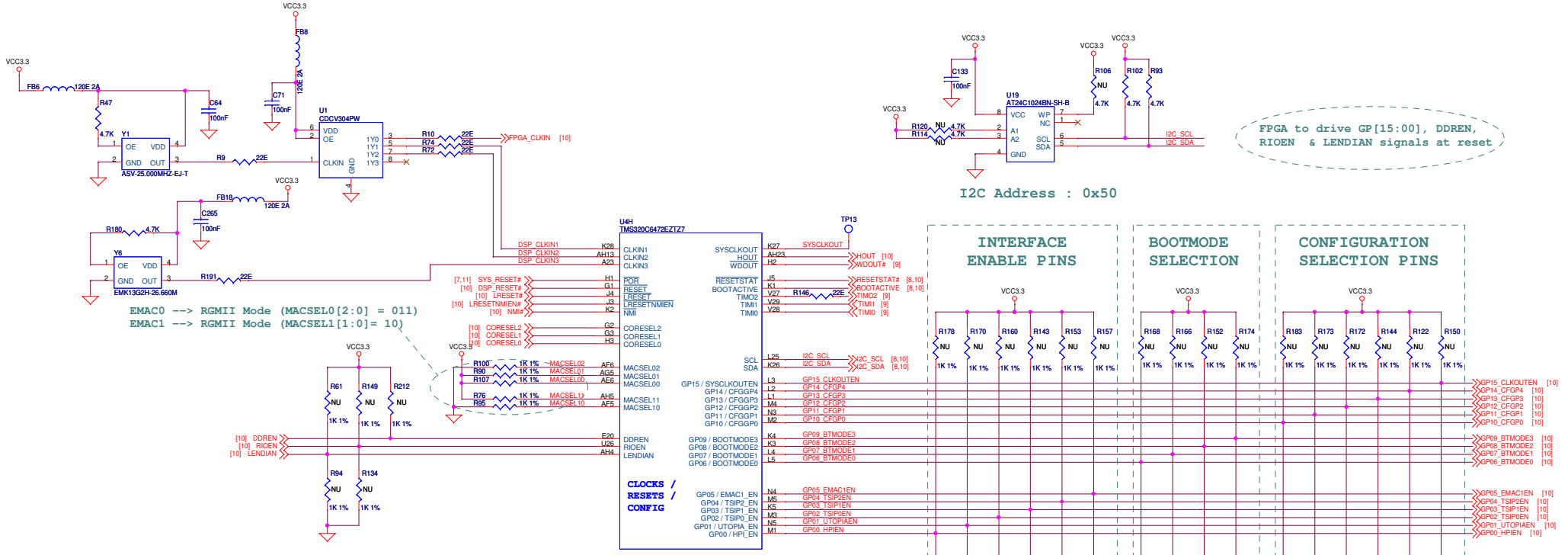
Project: TI_C6472EVM		Designed for TI by eInfochips
Title: Cover Sheet		Texas Instruments / eInfochips The Solutions People
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 1 of 12	

BLOCK DIAGRAM

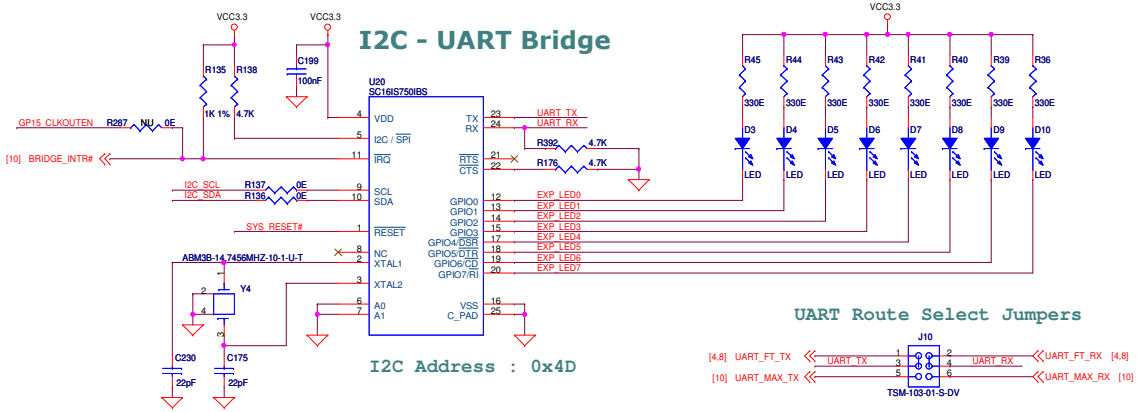


Notes:
1) GPIO[15:0] are multiplexed with configuration pins
2) RAM expandable to 512MB(128Mx16) DDR2-533

Project: TI_C6472EVM		Designed for TI by eInfochips
Title: System Block Diagram		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 2 of 12	



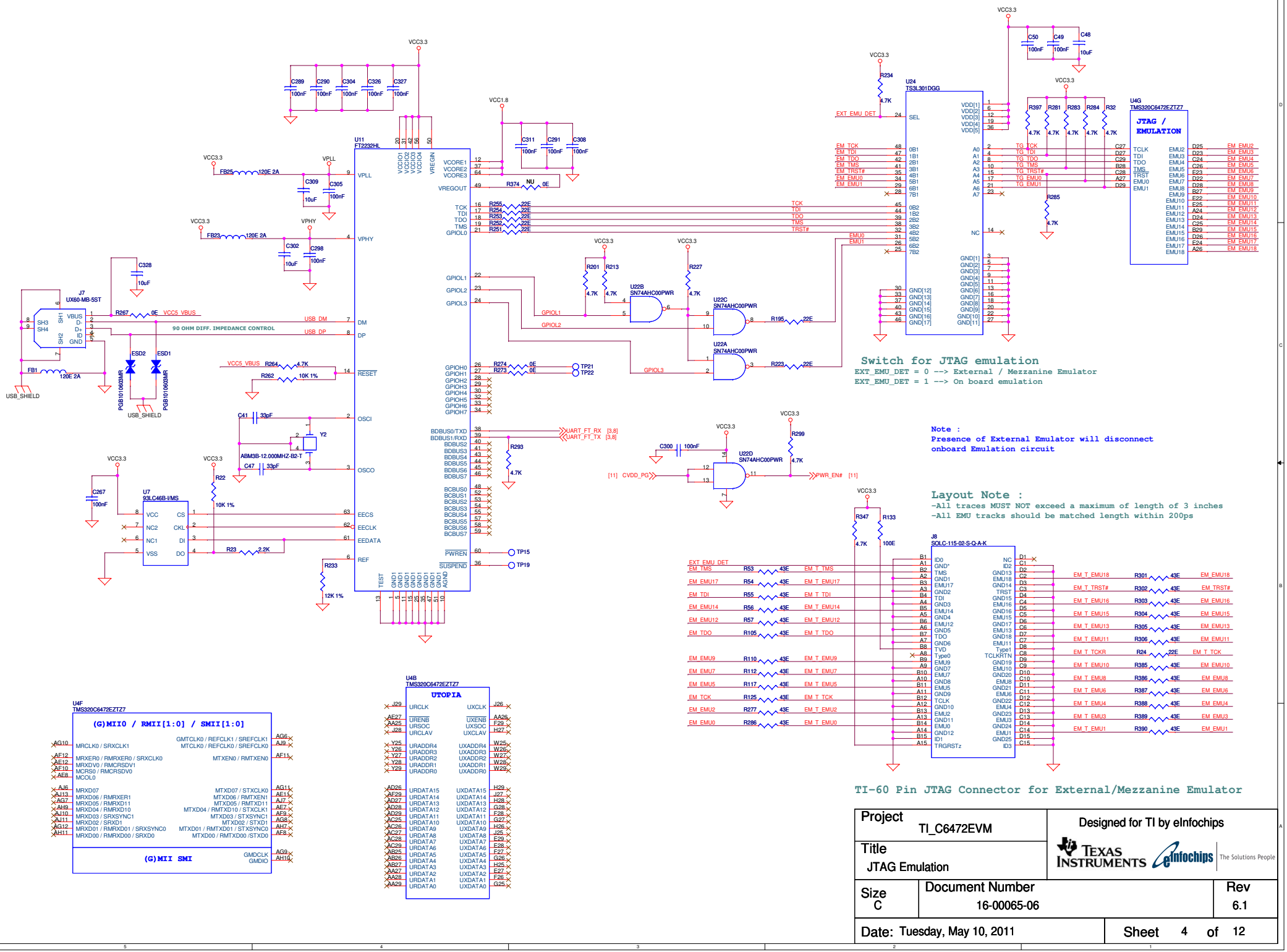
FPGA to drive GP[15:00], DDREN, RIOEN & LENDIAN signals at reset



BOOTMODE[3:0]	DESCRIPTION
0000 (0)	Immediate Boot
0001 (1)	Host (HPI) boot
0010 (2)	**Master I2C boot (address : 50H) -- Default**
0011 (3)	Master I2C boot (address : 51H)
0100 (4)	Slave I2C boot
0101 (5) - 1000 (8)	UTOPIA boot
1001 (9)	EMAC0 boot
1010 (10)	EMAC1 boot
1011 (11) - 1110 (14)	RIO[1:4]
1111 (15)	Reserved

J10.3 to J10.1 & J10.4 to J10.2: UART over USB Connector (Default)
J10.3 to J10.5 & J10.4 to J10.6: UART over 3-Pin Header J4

Project: TI_C6472EVM	Designed for TI by eInfochips	
Title: DSP Configuration, UART Bridge		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 3 of 12	


U11
FT2232HL
U4B
TMS320C6472EZTZ7
UTOPIA
U4F
TMS320C6472EZTZ7
(G)MII0 / RMII[1:0] / SMII[1:0]
(G)MII SMI
U4G
TMS320C6472EZTZ7
JTAG / EMULATION
U24
TS3L301DGG
J7
UX60-MB-5ST
J8
SOLC-115-02-S-Q-A-K
U7
93LC46B-I/MS
U22A
SN74AHC00PWR
U22B
SN74AHC00PWR
U22C
SN74AHC00PWR
U22D
SN74AHC00PWR
90 OHM DIFF. IMPEDANCE CONTROL
Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation
Note :
Presence of External Emulator will disconnect
onboard Emulation circuit
Layout Note :
-All traces MUST NOT exceed a maximum of length of 3 inches
-All EMU tracks should be matched length within 200ps
TI-60 Pin JTAG Connector for External/Mezzanine Emulator
Project
TI_C6472EVM
Designed for TI by eInfochips
Title
JTAG Emulation
Size
C
Document Number
16-00065-06
Rev
6.1
Date: Tuesday, May 10, 2011
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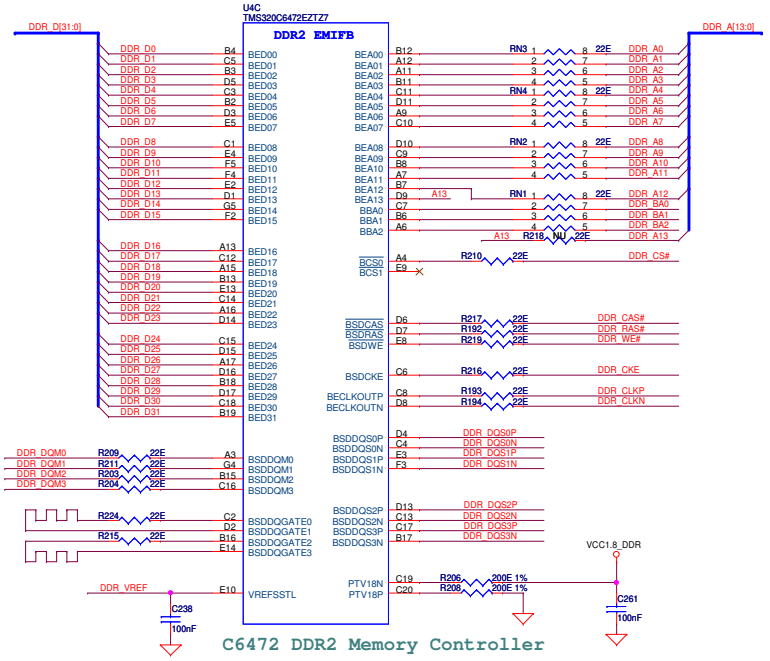
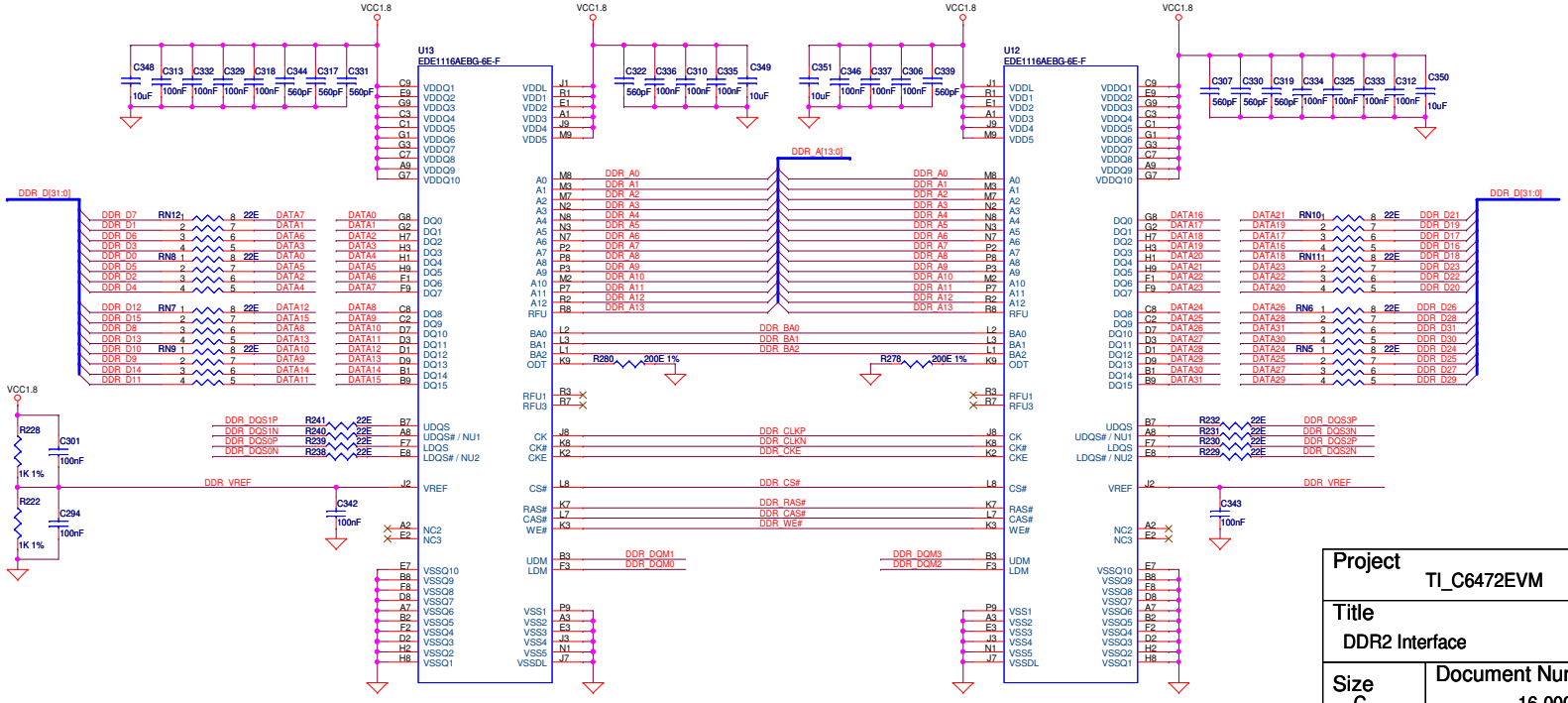
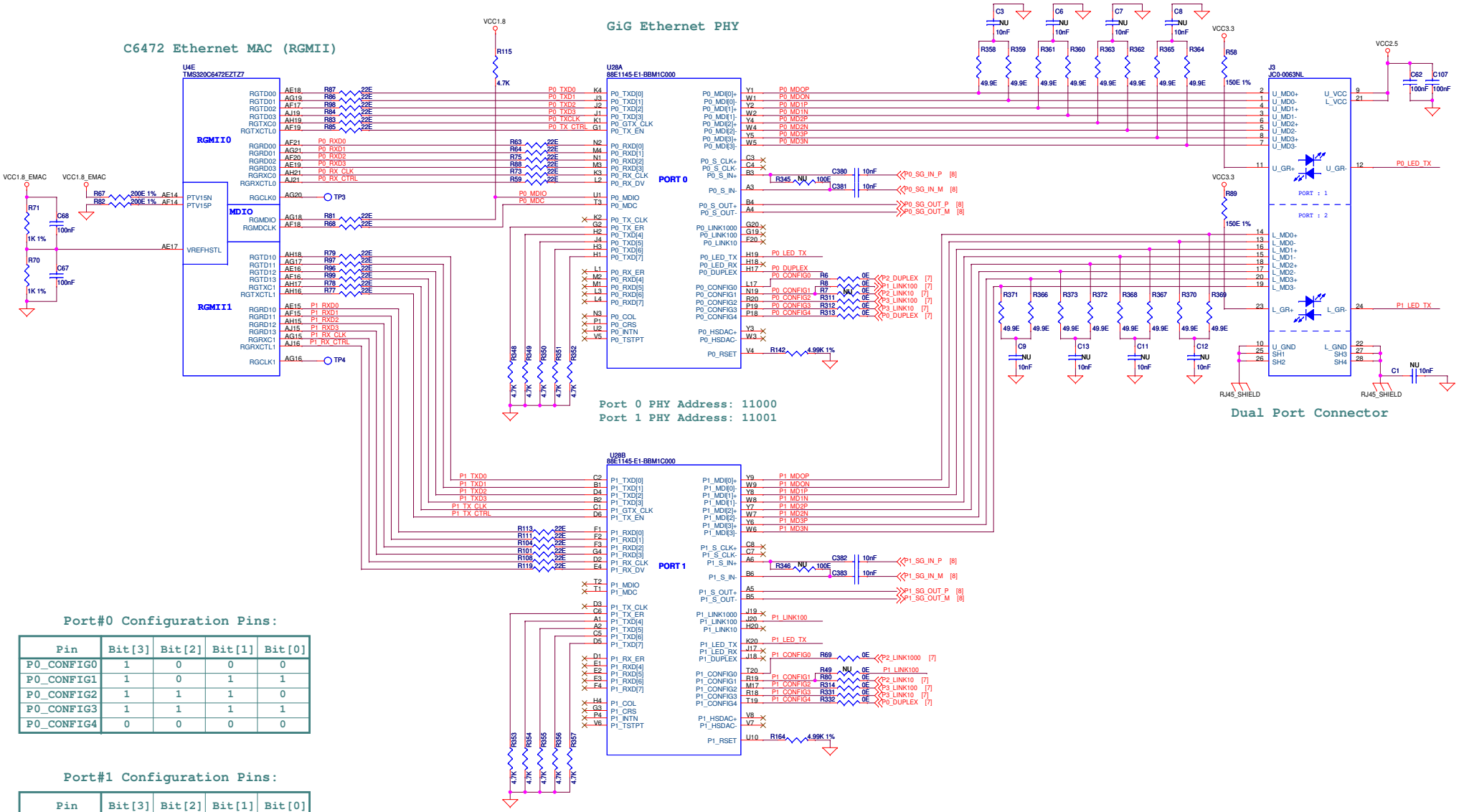


Supported Memories (84 FBGA) :

	256MB (128MB x 2)	512MB (256MB x 2)
Elpida	EDE1116AEBG-6E-F	
Micron	MT47H64M16HR-3	MT47H128M16HG-3



Project: TI_C6472EVM		Designed for TI by eInfochips
Title: DDR2 Interface		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 5 of 12	



Port#0 Configuration Pins:

Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P0_CONFIG0	1	0	0	0
P0_CONFIG1	1	0	1	1
P0_CONFIG2	1	1	1	0
P0_CONFIG3	1	1	1	1
P0_CONFIG4	0	0	0	0

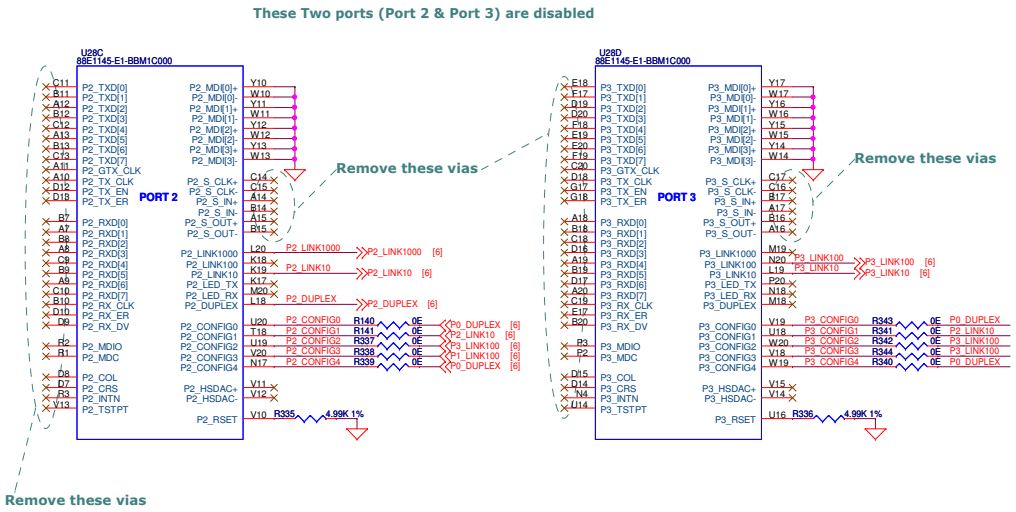
Port#1 Configuration Pins:

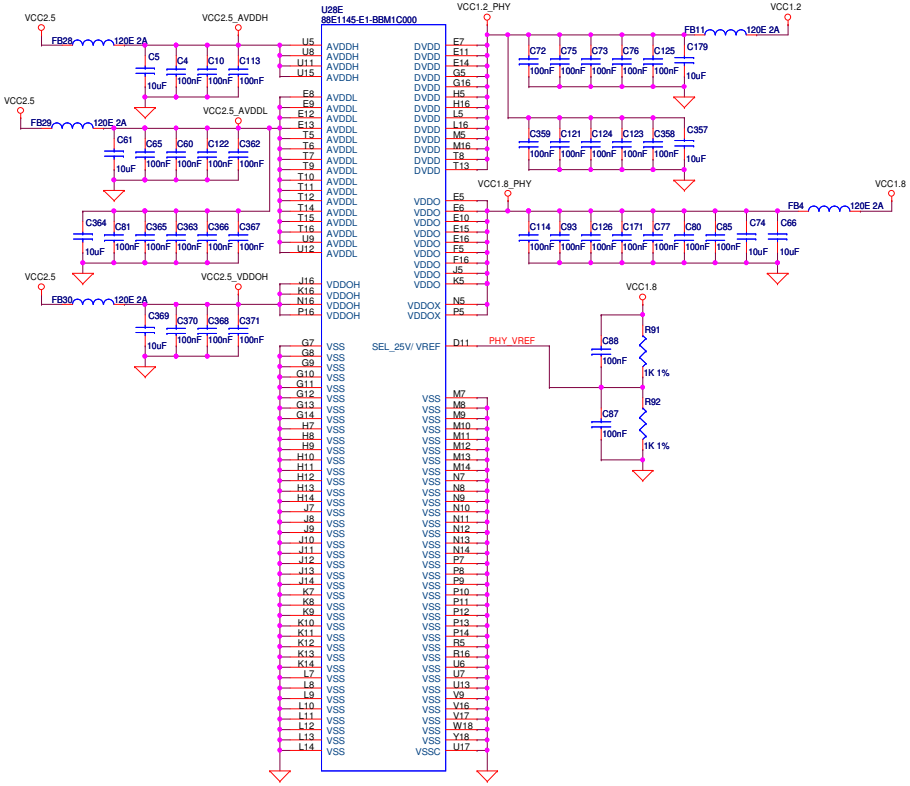
Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P1_CONFIG0	1	0	0	1
P1_CONFIG1	1	0	1	1
P1_CONFIG2	1	1	1	0
P1_CONFIG3	1	1	1	1
P1_CONFIG4	0	0	0	0

Note:

At Power On, Port0 will be "RGMII - SGMII" mode & Port1 will be "RGMII - Copper" mode through hardware configuration.

Project: TI_C6472EVM	Designed for TI by eInfochips	
Title: GiG Ethernet Interface # 01		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 6 of 12	



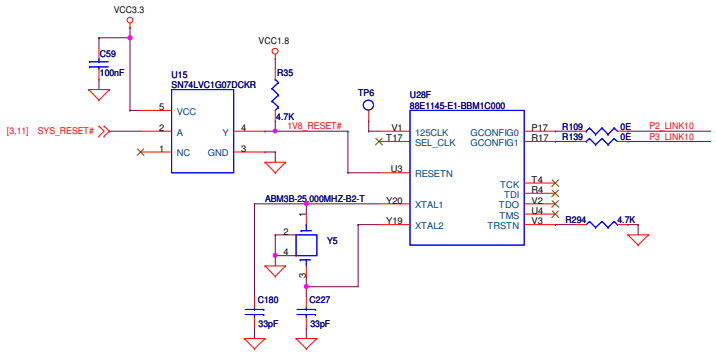


Port#2 Configuration Pins:

Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P2_CONFIG0	0	0	0	0
P2_CONFIG1	1	0	1	1
P2_CONFIG2	1	1	1	0
P2_CONFIG3	0	1	1	0
P2_CONFIG4	0	0	0	0

Port#3 Configuration Pins:

Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P3_CONFIG0	0	0	0	0
P3_CONFIG1	1	0	1	1
P3_CONFIG2	1	1	1	0
P3_CONFIG3	1	1	1	0
P3_CONFIG4	0	0	0	0



Global Configuration Pins:

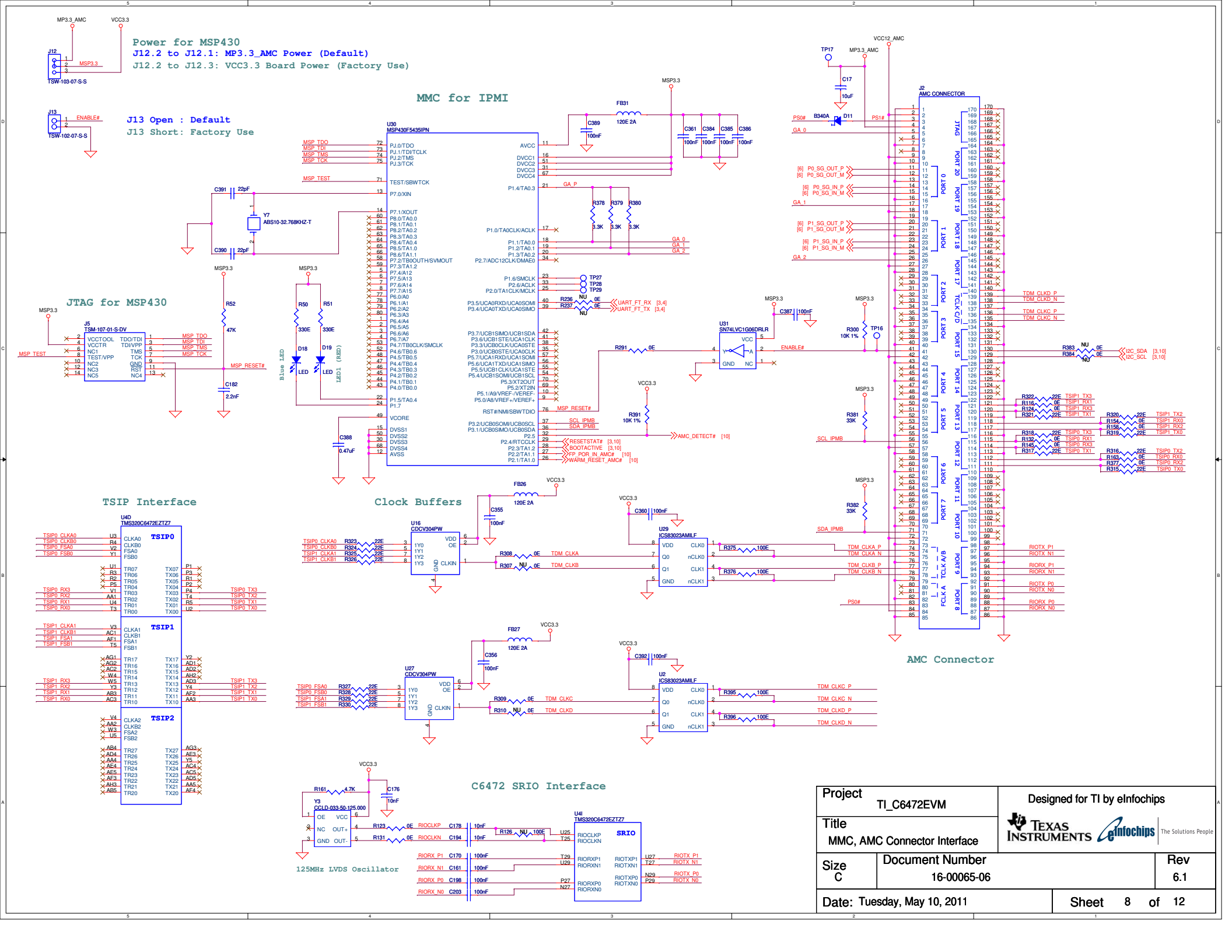
Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
GCONFIG0	1	0	1	1
GCONFIG1	1	1	1	1

Device Pins	Bit[3:0]
P3_LINK10	1111
P3_LINK100	1110
P3_LINK1000	1101
P3_DUPLEX	1100
P2_LINK10	1011
P2_LINK100	1010
P2_LINK1000	1001
P2_DUPLEX	1000
P1_LINK10	0111
P1_LINK100	0110
P1_LINK1000	0101
P1_DUPLEX	0100
P0_LINK10	0011
P0_LINK100	0010
P0_LINK1000	0001
P0_DUPLEX	0000
All Other	Reserved

Ethernet PHY Configuration Pins:

Pin	Bit[3]	Bit[2]	Bit[1]	Bit[0]
P[3:0]_CONFIG0	PHYADR3	PHYADR2	PHYADR1	PHYADR0
P[3:0]_CONFIG1	HWCFG_3	HWCFG_2	HWCFG_1	HWCFG_0
P[3:0]_CONFIG2	ANEG3	ANEG2	ANEG1	ANEG0
P[3:0]_CONFIG3	PHYADR4	ENA_XC	DIS_FC	DIS_SLEEP
P[3:0]_CONFIG4	Reserved	Reserved	SEL_TWSI	ENA_PAUSE
GCONFIG0	DIS_DTE	75/50 OHM	1/4 MDIO	DIS_125CLK
GCONFIG1	LED_TXblink	PowerDown	SIG_DET	INT_POL

Project: TI_C6472EVM	Designed for TI by eInfochips	
Title: GiG Ethernet Interface # 02		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 7 of 12	


Power for MSP430
J12.2 to J12.1: MP3.3_AMC Power (Default)
J12.2 to J12.3: VCC3.3 Board Power (Factory Use)
J13 Open : Default
J13 Short: Factory Use
MMC for IPMI
JTAG for MSP430
TSIP Interface
Clock Buffers
C6472 SRIO Interface
125MHz LVDS Oscillator
AMC Connector
Project
TI_C6472EVM
Designed for TI by eInfochips
Title
MMC, AMC Connector Interface
Size
C
Document Number
16-00065-06
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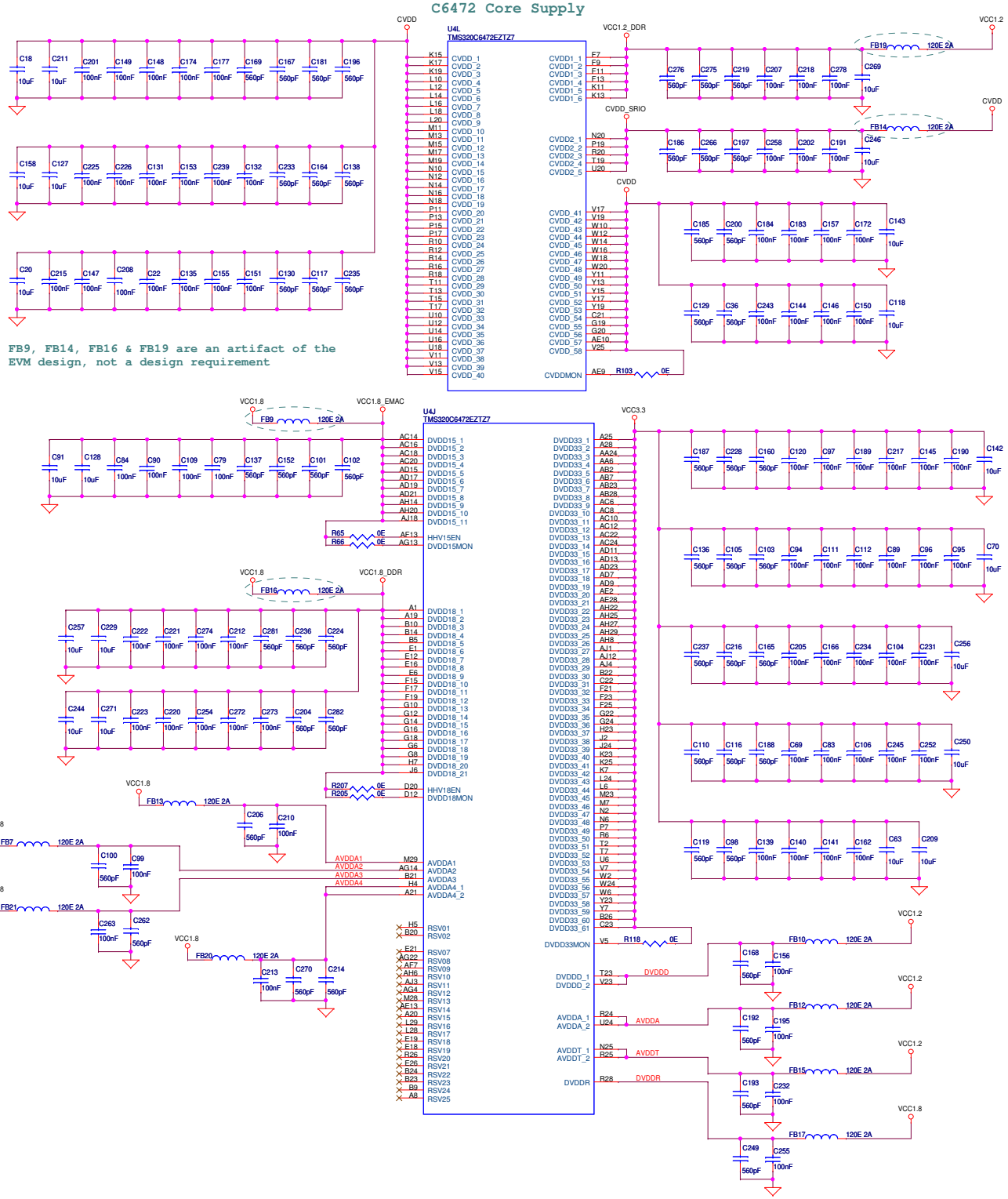
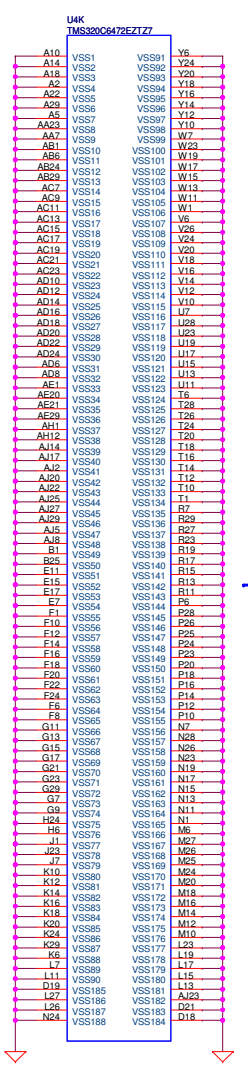
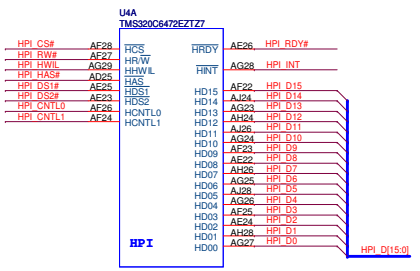
C6472 Core Supply



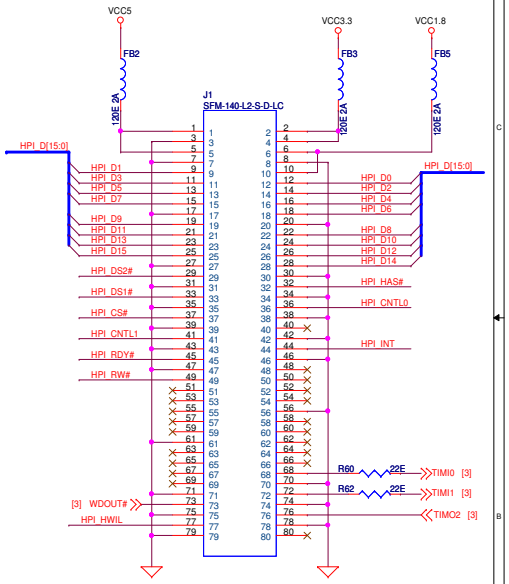
C6472 Ground



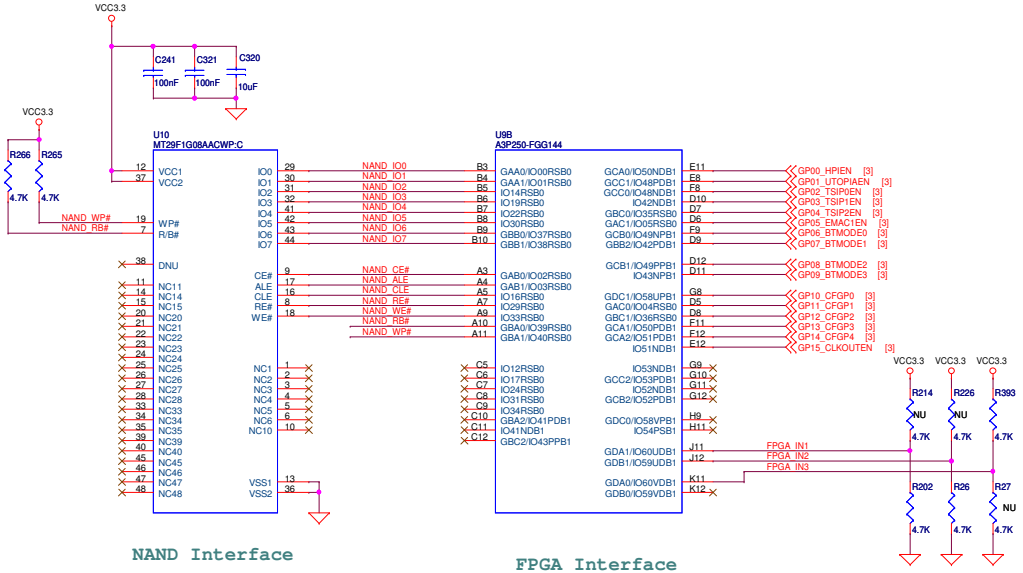
C6472 HPI Interface



HPI DC Connector

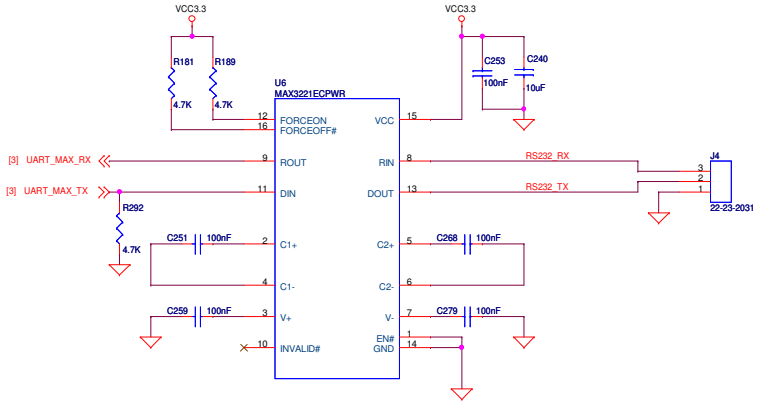


Project: TI_C6472EVM	Designed for TI by eInfochips	
Title: HPI_DSP Power Supply		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 9 of 12	



NAND Interface

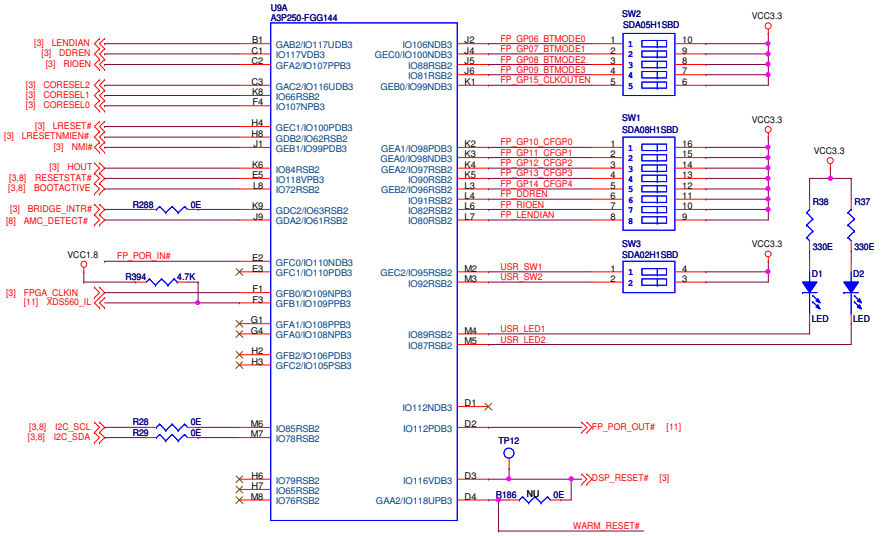
FPGA Interface

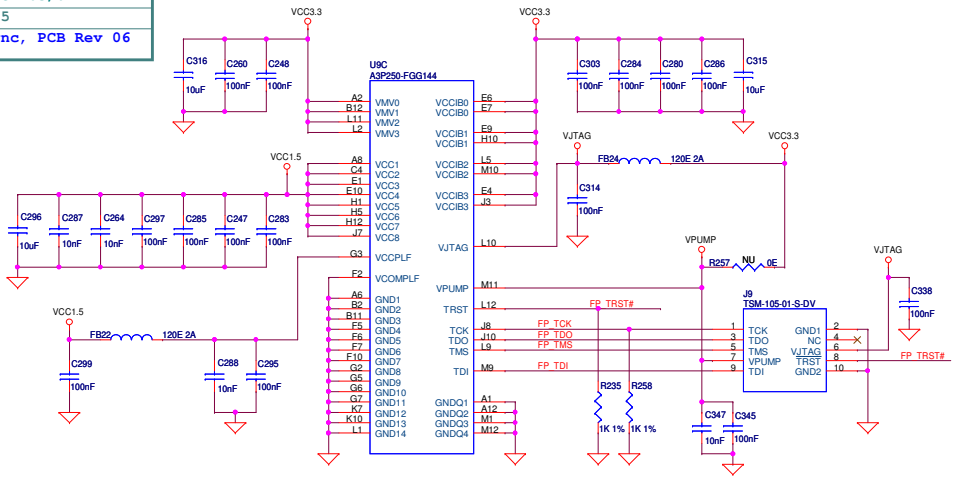


Size	128MB
Device ID	0x2C
Page Size	(2048 + 64) Byte
Block Size	64 Pages

Board Build Identification

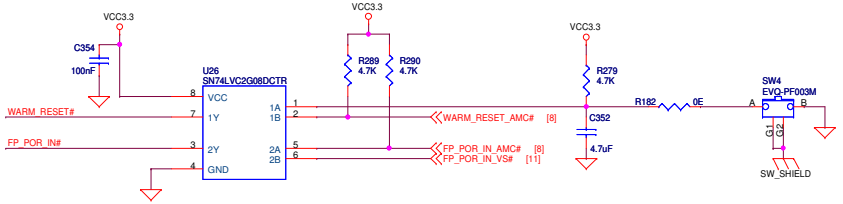
[K11:J12:J11]	Description
000	Proto-type,PCB Rev 01
001	AMC-TSIP/I2C Changes,PCB Rev 02
010	SGMII Support Added,PCB Rev 03/04
011	IPMI MMC Added, PCB Rev 05
100	TCLKC/D used for Frame Sync, PCB Rev 06

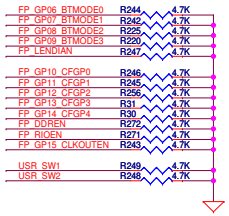




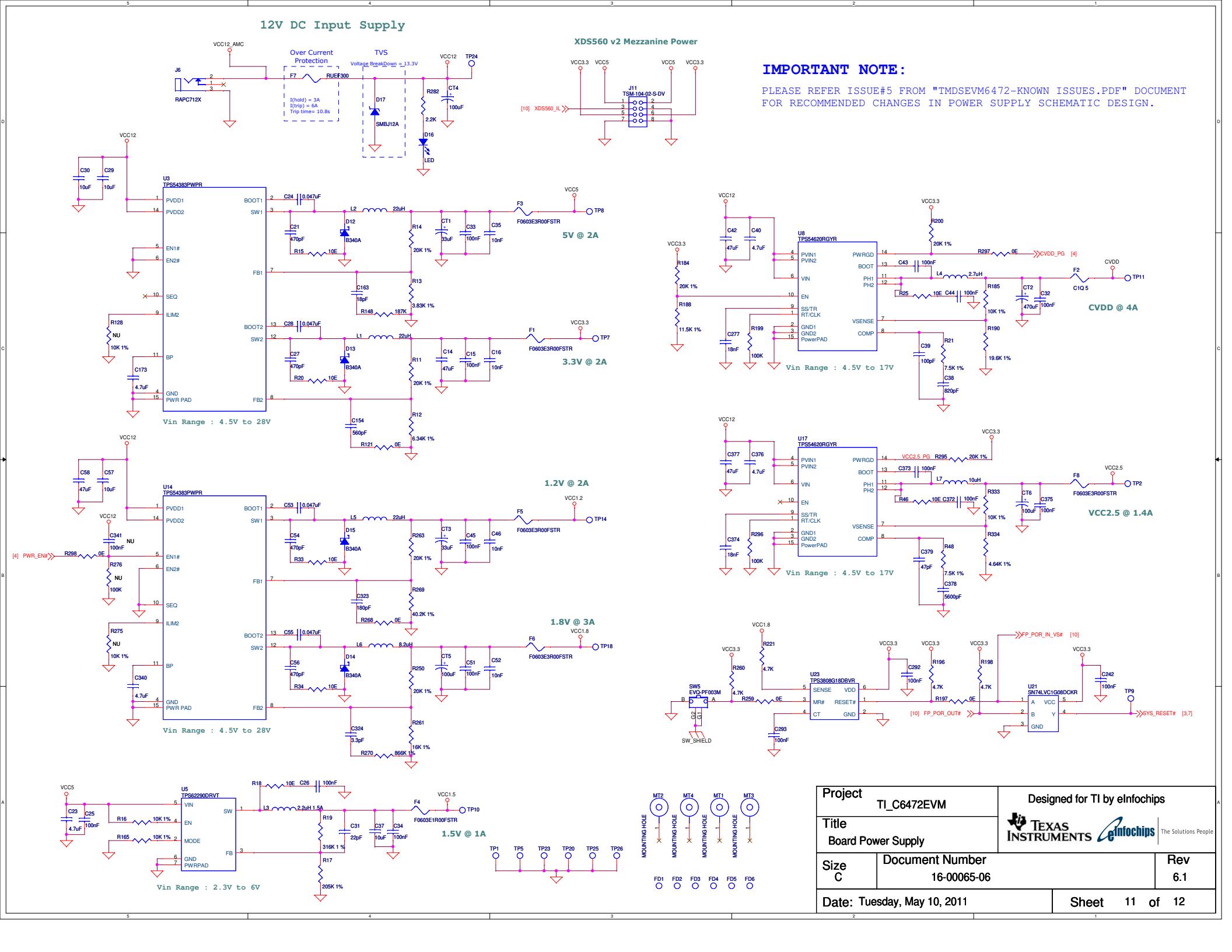
FPGA Power

FPGA JTAG Connector





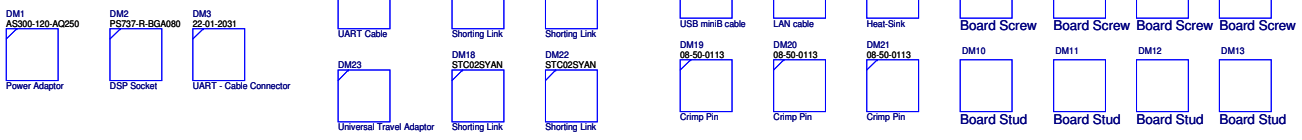
Project: TI_C6472EVM		Designed for TI by eInfochips	
Title: FPGA - NAND Flash Interface			
Size: C	Document Number: 16-00065-06		Rev: 6.1
Date: Tuesday, May 10, 2011		Sheet 10 of 12	


12V DC Input Supply
Over Current Protection
TVS
Voltage BreakDown = 13.3V
I(hold) = 3A
I(trip) = 6A
Trip time= 10.8s
RAPC712X
RUEF300
SMBJ12A
LED
XDS560 v2 Mezzanine Power
TSM-104-02-S-DV
XDS560_IL
IMPORTANT NOTE:
PLEASE REFER ISSUE#5 FROM "TMDSEVM6472-KNOWN ISSUES.PDF" DOCUMENT FOR RECOMMENDED CHANGES IN POWER SUPPLY SCHEMATIC DESIGN.
TPS54383PWPR
5V @ 2A
3.3V @ 2A
Vin Range : 4.5V to 28V
TPS54620RGYR
CVDD @ 4A
Vin Range : 4.5V to 17V
1.2V @ 2A
1.8V @ 3A
VCC2.5 @ 1.4A
TPS62290DRVT
1.5V @ 1A
Vin Range : 2.3V to 6V
TPS3808G18DBVR
SN74LVC1G08DCKR
SW_SHIELD
MOUNTING HOLE
Project
TI_C6472EVM
Designed for TI by eInfochips
Title
Board Power Supply
Size
C
Document Number
16-00065-06
Rev
6.1
Date: Tuesday, May 10, 2011
Sheet 11 of 12

TI_C6472EVM - REVISION HISTORY

PCB REV.	SCH. REV.	CHANGE DESCRIPTION	DATE	AUTHOR
1.0	Issue 1.0	- Released for Fabrication of PCB ver1.0 (Proto-1)	06AUG2009	eInfochips
	Issue 1.1	- Updated BOM for second batch of 22 boards	09SEP2009	eInfochips
2.0	Issue 2.1	- Released for Fabrication of PCB ver2.0 (Production batch 1)	24SEP2009	eInfochips
3.0	Issue 3.2	- Released for Fabrication of PCB ver3.0 (SGMII Proto)	27OCT2009	eInfochips
4.0	Issue 4.2	- Released for Fabrication of PCB ver4.0 (SGMII Production)	22JAN2010	eInfochips
5.0	Issue 5.2	- Released for Fabrication of PCB ver5.0 (IPMI feature - Proto + Production)	18MAY2010	eInfochips
	Issue 5.3	- R126 changed to NU (Not Used) from Used - Removed U25 from I2C address table at sheet 1 - U11.28 changed to NC (No Connect) - Note on sheet 3 changed from "UART over 3-Pin Header J5" to "UART over 3-Pin Header J4" - Added "Universal Travel Adaptor" as dummy part. -- WEB Release for V05 batch	12JULY2010	eInfochips
6.0	Issue 6.0	- Pull down added on UART inputs lines - Pull up added on "TG_TCK" net - Board build identification changed from 2 bit to 3 bit - U2 (ICS83023AMILF) added	04SEP2010	eInfochips
	Issue 6.1	- D18 Part # changed to LNJ952W8CRA1 (old part is obsolete) - Added note in power supply page	10MAY2011	eInfochips

Dummy Components



Project: TI_C6472EVM		Designed for TI by eInfochips
Title: Revision History & Dummy Parts		
Size: C	Document Number: 16-00065-06	Rev: 6.1
Date: Tuesday, May 10, 2011	Sheet 12 of 12	